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DESIGN A CIRCUIT LEVEL LOW LEAKAGE AND ROBUST FLIP LECTOR APPROACH FOR SRAM CELL

DEEPAK MITTAL [1], V.K. TOMAR [2]

[1]Assistant Professor, Department of Electronics and Communication Engineering, GLA University Mathura-281406, Uttar Pradesh, India.
[2]Professor, Department of Electronics and Communication Engineering, GLA University Mathura-281406, Uttar Pradesh, India.

ABSTRACT

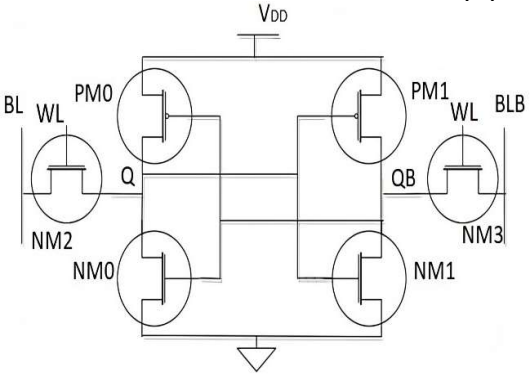
In static random access memory (SRAM) cells, leakage power, stability, and speed have become significant challenges with the scale-down of technology. This paper presents a proposed Flip LECTOR approach. In the LECTOR approach, a leakage-controlled transistor (LCT) is always near its "cut-off" voltage for any input supply. In the GALEOR approach, gated transistors NMOS and PMOS are unsuitable for passing the VDD and ground at pullup (PUN) and pulldown (PDN), respectively. In MTCMOS, gated transistors may fail the gates, which reduces the noise margin. Also, due to additional mask layers, the fabrication process becomes complex. Hence, due to the above approaches, the operation of the 6T SRAM cell was vitiated. There is also signal quality contention, but this method does not have these problems because the adjacent LCT is always close to its linear voltage when one of the transistors in the SRAM cell is either PMOS or NMOS and "ON." LCT increases the resistance, which reduces leakage power. When compared to a 6T SRAM, LECTOR, GALEOR, and MTCMOS at 1V, the proposed method reduces the leakage power 2.55×, 5.84×, 1.08×, and 1.52× during read operation respectively. It is also 1.57×, 24×, and 1.15× improved during the write operation. The read delay is 3.82× and 3.83× smaller than that of LECTOR and GALEOR. The write delay is 1.21×, 1.26×, and 1.37× less than that of LECTOR, GALEOR, and MTCMOS. Proposed approach WSNM is 1.92×, 1.03×, 1.78×, and 1.43× better than 6T SRAM, LECTOR, GALEOR, and MTCMOS.

Keywords: *SRAM cell, leakage power dissipation, stability, power delay product, slew rate, Flip LECTOR Approach.*

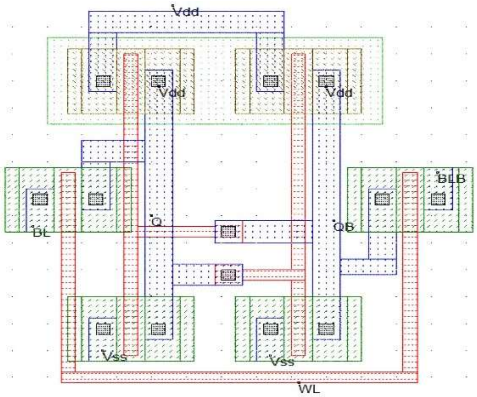
1. INTRODUCTION

An increasing need of battery operated portable digital systems requires shrinking device size and supply voltage scaling [1] which results in decrease of voltage difference between supply voltage and transistor threshold voltage. It causes a change in stability which becomes a critical challenge in low-power SRAM cell design [2]. Device scaling also results in several issues like sub-threshold current, gate-induced drain leakage, and drain-induced barrier lowering [3]. In deep submicron design, leakage current flows across the devices in standby mode and increases with an increase in temperature. Thus, the leakage current becomes a significant part of total power dissipation [4]. In VLSI circuits, power dissipation significantly affects both cost and functionality. Consequently, power dissipation is an important consideration for CMOS VLSI technology development [5]. Device and voltage scaling restrict the ability to obtain low-power circuits and system-level approaches [6-8]. The battery's lifespan is limited, and even though battery technology has come a long way, like with high-capacity reusable lithium-ion cells, there may be a small change in the near future. The only way to lower power consumption under these conditions is to use creative low-power circuit design techniques. Furthermore, in these techniques leakage power management strategies must be used to prevent needless power dissipation while the circuit or any component elements are not in use [9-11]. Portable devices must also have a fast-functioning main memory to perform high-speed computation operations. It can be fulfilled by utilizing SRAM as cache memory in the system on chip devices [12-14]. In this research, the proposed Flip LECTOR approach possesses lesser delay, increased stability in active mode, and lower leakage power in standby mode compared to other cells. The rest of the paper

is laid out as follows: Section 2 presents how to build a traditional 6T SRAM cell using industry-standard methods. Section 3 depicts the design of an SRAM cell using leakage reduction hybrid approaches. The SRAM cell that has been proposed is being explored in Section 4. In Section 5, the simulation results are summarized and visually analyzed. Section 6 contains the conclusion of the paper.



(a)



(b)

Figure 1: Traditional 6T SRAM cell (a) Schematic, (b) Layout

2. TRADITIONAL 6T SRAM CELL

A 6T SRAM cell schematic and layout are shown in Fig1. Two-pass transistors, two pull-down transistors (NM0 and NM1), and two PM0 and PM1 pull-up transistors form a 6T SRAM cell (NM2, NM3). The word-line inputs control the gates of the pass transistors (WL). The cell can be accessed for reading and writing when the word line is high due to its connection with the BL and BLB. The power used during variations in output is called "dynamic power dissipation." Cells are unreachable for reading or writing while the word line is zero [2].

In this instance, the power being measured is static power dissipation. For writing to be successful, there must first be a write driver that searches for data and then gives permission for it to be written into the cell. A schematic illustrating this write driver is shown here. It's merely a NOT gate with data inputs and writing capability. When the writer reads, their capacity to produce writing is diminished. The BL and BLB must first be charged to a specific voltage level before the reading can begin. It ensures that the voltage on both bit lines is the same. The pre-charge circuit is handling the pre-charge at this point. The voltage difference between the nodes of the access transistor and the value stored in the SRAM cell output causes the capacitor at one end to discharge after it has been pre-charged. It occurs because the capacitor holds the value that was previously stored. The voltage differential causes this to deplete the capacitor at the opposite end (Q vs. QB). A differential amplifier known as the sense amplifier measures and amplifies the voltage difference between BL and BLB.

3. LEAKAGE REDUCTION APPROACHES FOR SRAM CELL

In this section, we have examined several SRAM cells using leakage reduction approaches to reduce static and leakage power consumption.

3.1 SRAM Cell GALEOR Approach

In the GALEOR approach, the output terminal and pull-down network (PDN) are sequentially linked to one additional transistor. In contrast, the pull-up network (PUN) and the output terminal are connected to the other transistor. Due to the additional transistors' connections to one another, the cut-off region is close to them. According to Ohm's law, this increases the path resistance from the source to the ground, which results in a severe loss of control. However, one of the extra implanted transistors is still relatively close to the voltage that turns it off, which raises issues about the GALEOR method's capability to create good-quality signals. The GALEOR approach is a self-controlling leakage device since the extra transistors are already biased [14]. The schematic and layout of a GALEOR-compatible SRAM cell are shown in Fig 2.

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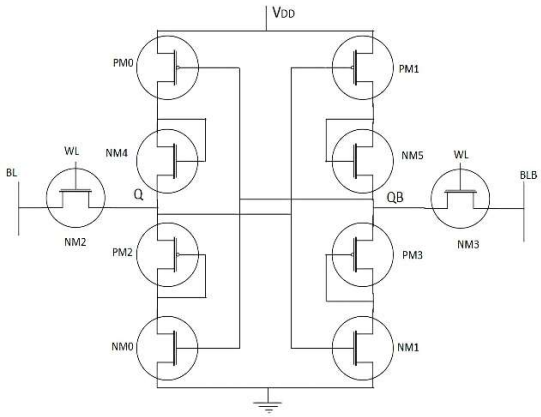
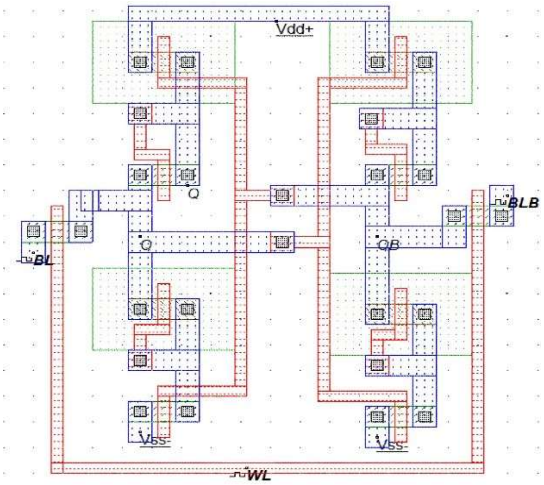


(a)

The cut-off region is always within reach because of how the transistors (NM4, NM5, PM2, and PM3) are connected. In active mode, the line "WL" is set to a high voltage, enabling the process of reading and writing data on the SRAM cell. "Dynamic power" is the term used to describe the power measured while a device is in active mode.



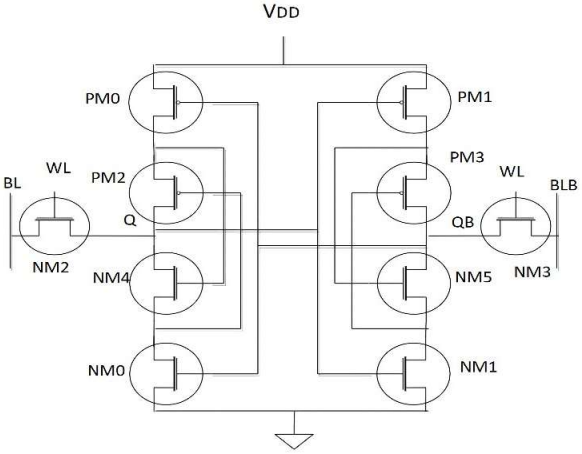
(b)

Figure 2: SRAM Cell GALEOR Approach: (a) Schematic, (b) Layout

During the standby mode of the word line "WL," when set to a low value, no read or write operations are allowed in the specific cell. The increased resistance, resulting from the presence of more OFF transistors, leads to a reduction in leakage current. In this instance, the calculated power remains constant. The nodes labelled "BL" and "BLB" serve as input terminals, whereas the nodes labelled "Q" and "QB" function as output terminals.

3.2 SRAM Cell LECTOR Approach

Two additional transistors are connected in series with the PUN and PDN of the LECTOR technique, one between each of them and the output terminal [17]. The extra transistors (one p-MOS and one n-MOS) are linked to maintaining the cut-off region. Leakage is significantly decreased due to the higher route resistance from the supply to the destination. However, LECTOR is afflicted by signal quality problems caused by low rise and fall time values. The leaking device is self-controllable due to a higher number of internally biased transistors than externally biased ones. Fig.3 are the schematic and layout representations of an SRAM cell that employs the LECTOR methodology.



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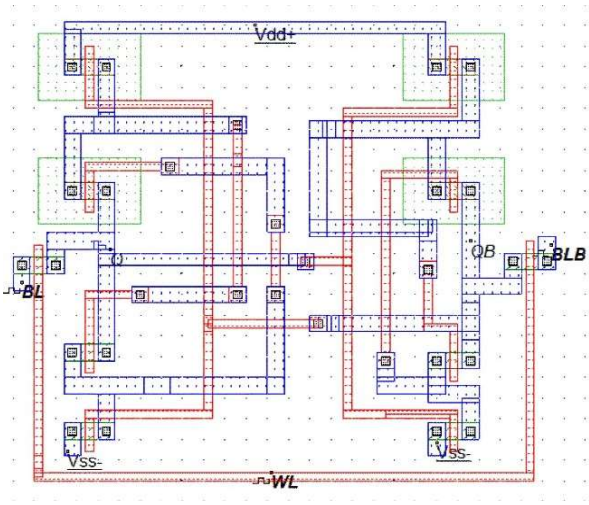

(b)

Figure 3: SRAM Cell LECTOR Approach: (a) Schematic, (b) Layout

The extra transistors (PM2, PM3, NM4, and NM5)

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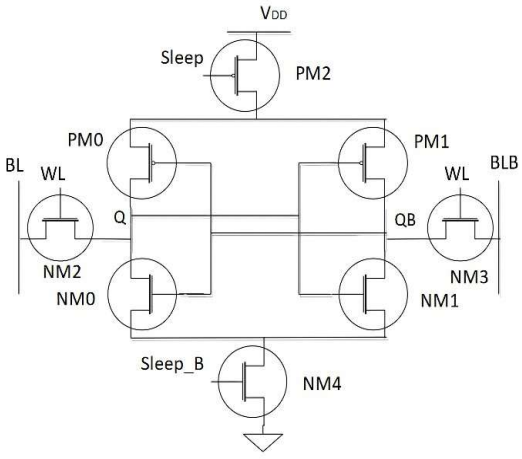
are interconnected to maintain their proximity to the cut-off point. During the active state of the SRAM cell, the word line "WL" is set to a high voltage level, which allows for both data writing and reading operations. This mode is known as "dynamic power". Because the word line "WL" is set to zero and all transistors are switched off in standby mode, leakage current is reduced, but resistance increases. In this mode, static power is used. "BL" and "BLB" are inputs, whereas "Q" and "QB" are outputs.

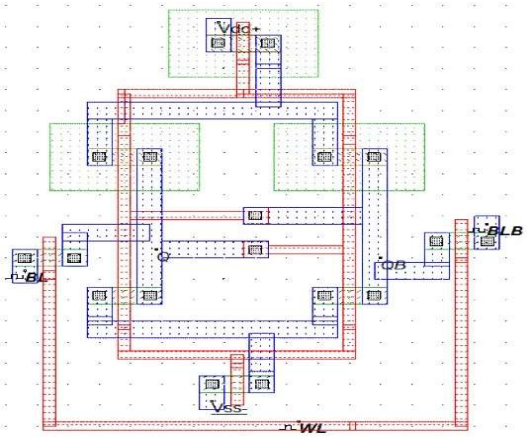
3.3 SRAM Cell Power Gating (MTCMOS) Approach

The power supply is isolated from the pull-up network, and the two high threshold voltage (V_T) sleep transistors are turned off during standby mode, which reduces the amount of leakage power dissipated during this state. A circuit loses information when sleep transistors are turned off [6-8]. Fig. 4 is the conceptual diagram and layout of an MTCMOS-produced SRAM cell.

The "Sleep" and "Sleep B" inputs activate the sleep transistors (PM2, NM4). In active mode, the settings for "WL" and "Sleep B" are set to high, while the setting for "Sleep" is set to low. When the SRAM cell is linked to the ground terminal and the power supply voltage via the sleep transistors, it can write and read data (PM2, NM4). The power accumulated in this state is referred to as dynamic power. While in standby mode, "Sleep" is set to high, while "Word Lines (WL)" and "Sleep B" are both deactivated. The sleep transistors (PM2, NM4) are deactivated, reducing the amount of leakage power. The cell is on standby mode, and the measured power is static. "BL" and "BLB" are the inputs, while "Q" and "QB" are the outputs.



(a)



(b)

Figure 4: SRAM Cell MTCMOS Approach (a) Schematic, (b) Layout

4. PROPOSED SRAM CELL FLIP LECTOR APPROACH

The proposed Flip LECTOR approach includes:

•Two p-MOS transistors between the PUN and output terminal.

•Two n-MOS transistors between the PDN and output terminal.

•Four extra transistors are linked in series between the PDN and PUN.

Two additional pull-up p-MOS transistors, PM2 and PM3, have their drains linked to the pull-down n-MOS transistors, NM2 and NM3, respectively. Consequently, when NM3 is activated, PM2 is also activated, and vice versa. Similarly, two additional pull-down n-MOS transistors, NM0 and NM1, are connected to the drains of pull-up p-MOS transistors, PM0 and PM1, such that pull-down n-MOS transistors NM0 become "on" when pull-up transistor PM1 becomes "on." Similarly, pull-down transistor NM1 becomes "on" when pull-up transistor PM0 becomes "on." It showed that when Q = "0" and QB = "1," the PM0 and NM2 transistors get "on," and when the NM2 transistor becomes "on," the PM3 transistor also becomes "on." As a result, the proposed Flip Lector method operates in the same manner as a typical SRAM cell. Leakage considerably decreases due to increased route resistance between the supply and the ground. On the other hand, Flip LECTOR does not suffer from signal quality. There are more transistors within the Flip LECTOR than outside; it is a self-controlled leakage device. Fig. 5 depicts a schematic and layout of an SRAM cell using the Flip LECTOR approach.

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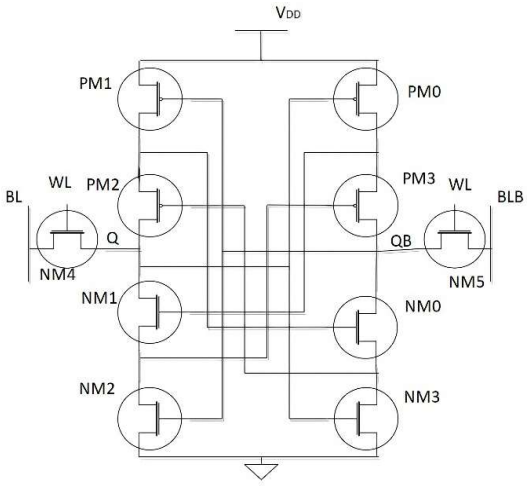
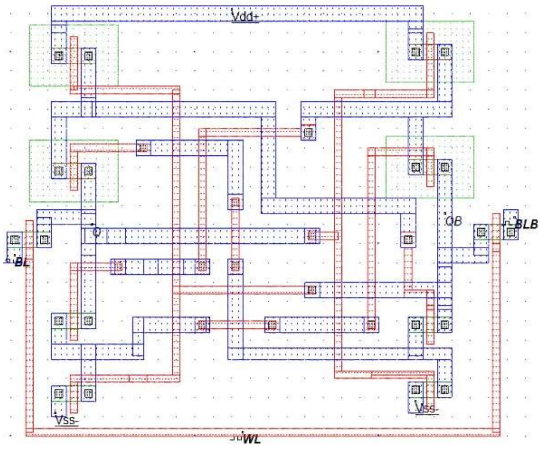


(a)

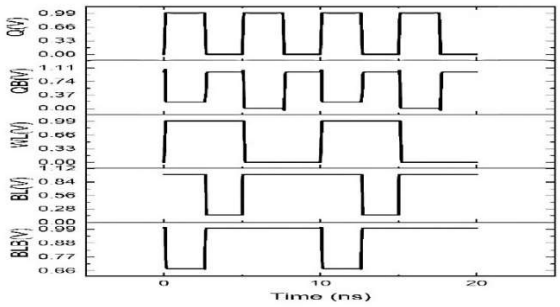
They are coupled so that the additional transistors PM2, PM3, NM1, and NM0 remain close to the linear voltage. When the word line "WL" is set to a high level, the SRAM cell's active mode is activated, allowing it to read and write data. The word line "WL" is set to zero, and all transistors in standby mode are switched off, raising resistance and decreasing leakage current. Inputs are "BL" and "BLB," while outputs are "Q" and "QB."



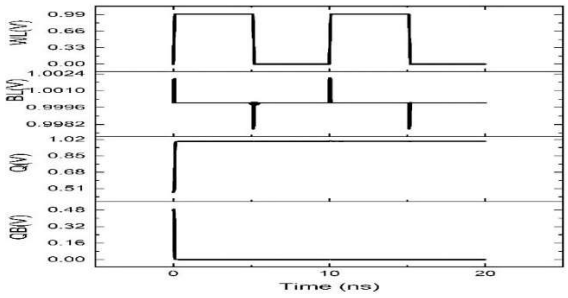
(b)

Figure 5: Proposed SRAM Cell Flip LECTOR Approach (a) Schematic, (b) Layout

The proposed Flip LECTOR approach's read and write operation waveforms are shown Fig. 6. In the read operation, when "Q" is equal to "1" and "QB" is similar to "0," the word line (WL) is also high "logic 1," so the "Q" value reflects on "BL" and the "QB" value reflects on "BLB." "BL" and "BLB" pass through a sense amplifier. This sense amplifier calculates the difference voltage of "BL" and "BLB" and provides the logic value if this value is equal to or more than 0.5V, so it reads as the logic "1"; if this value is less than 0.5V, so it reads as the logic "0" in 45nm technology. In the write operation, "BL" is logically "1" because the pre-charge circuit is "ON" and load capacitors are fully charged up, and at the same time, on the opposite side, "BLB" is connected to the ground. When the word line "WL" is high "logic 1," the "BL" value reflects on "Q," and "Q" becomes logically "1," the same as on the opposite side, where the "BLB" value reflects in "QB." This whole process is known as the write operation. The different parameter specifications were observed when simulating the approaches of SRAM to achieve optimum outputs. Access transistors should be stronger than pull-up transistors for stable read-and-write operation. So, the pull-up ratio should be greater than 1, which is the ratio of the width of access and pull-up transistor. Same as the pull-down transistor should be strong enough than the access transistor. So, the cell ratio should be greater than 1, which is the ratio of the width of the pull-down and access transistor.



(a)



(b)

Figure 6: SRAM Cell Flip LECTOR Approach operation waveforms (a) Read, (b) Write

5. SIMULATION RESULTS

The Cadence Virtuoso tool creates SRAM cells using 45 nm technology. Calculations for read and write operations include power dissipation, leakage power dissipation, delay measurement, power delay

product, settling time, and slew rate have been performed which are shown in tables 1 to 10 for 0.6 V to 1V. Measured data was used to determine the power delay product. To determine the read static noise margin (RSNM) and the write static noise margin (WSNM), the butterfly curves are produced by voltage transfer characteristics. To get the inverter RSNM and WSNM values of the SRAM cell, we measure the length of the longest side of the biggest square that can fit inside the lobes of butterfly curves. This length is the maximum size of the square that the butterfly curves can accommodate. Area comparison of SRAM Cell using various approaches are shown in table 7.

5.1 Read and Write Power Dissipation

In read and write operation both access transistors switch on when a read operation causes the word line to go high. The pre-charge circuit charges the capacitors in the BL and BLB. When Q is 1, and QB is 0, the BLB capacitor discharges through the pull-down path of the inverter circuit when the BLB value is 0. BL and BLB lines connect to the differential amplifier to read the data [13-16]. The differential amplifier detects the input difference and outputs the correct signal. The read power dissipation occurs when the SRAM cell consumes during this read operation. A graphical representation of read power dissipation is shown in Fig. 7 (a). When the supply voltage is reduced, the read power dissipation reduces [17-19]. The proposed Flip LECTOR method read power dissipation is 18.73×, 3.8×, and 9.67× less than conventional 6T SRAM cells, the LECTOR and GALEOR approaches, respectively, and 1.28× higher than the MTCMOS approach for 1 volt supply. At the time of the write operation, the word line becomes high again, and BL and BLB serve as input lines. The output lines Q and QB are used. Assume that Q is 0 and QB is 1 [20-23]. During writing, BLB is connected to the ground so that QB will be discharged through the ground of BLB by the access transistor, and QB will become '0'. This '0' turns the Q into a '1'. This approach consumes power and is called write power dissipation [26]. The proposed Flip LECTOR technique write power dissipation is 3.07× less as compared to the GALEOR technique and 1.54×, 2.41× and 1.57× higher than conventional 6T SRAM cell, LECTOR and MTCMOS approaches. Total Power dissipation in CMOS circuit can be calculate by the equation (1). A graphical representation of write power dissipation is shown in Fig. 7 (b). When Q = 1 and QB = 0, in this case PM3 transistor operates in cutoff region, and when Q=0 and QB= 1, in this case PM2 transistor operates in cutoff region so the resistance increases in the path, due to this power dissipation reduced.

Table 1. Comparison of SRAM Cell for read operation using various approaches at input voltage 0.6 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Read Power Dissipation (µw)	0.686	0.53	0.336	0.213	**0.197**
Leakage Power dissipation during Read (pw)	11.16	15.10	7.58	9.419	**6.978**
Read Delay (ps)	**136.8**	513.6	264.8	660.2	457.7
Rise Time (ps)	49.5	9.754	56.4	9.90	**9.779**
Fall Time (ps)	130.9	**38.58**	83.66	55.8	65.74
Power Delay Product (aJ)	93.89	272.20	**88.97**	140.62	**90.16**
Settling Time (ns)	19.99	15.19	19.99	15.19	**15.20**
Slew Rate (GHZ)	0.664	**10.89**	0.702	10.72	**10.74**
Read Static Noise Margin (RSNM) Volts	0.152	0.240	0.045	**0.403**	**0.32**

Table 2. Comparison of SRAM Cell for write operation using various approaches at input voltage 0.6 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Write Power Dissipation (nw)	**2.878**	4.183	7.528	2.888	4.81
Leakage Power dissipation during Write (pw)	111.922	7.279	63.93	8.905	**6.967**
Write Delay (ps)	235.5	**50.73**	291.3	504.9	403.5
Rise Time (ps)	107.9	**9.987**	27.54	16.1	248.3
Fall Time (ps)	64.07	**7.408**	89.64	94.2	71.11
Power Delay Product (aJ)	0.677	**0.212**	2.192	1.458	1.94
Settling Time (ps)	285.4	168.4	**162.8**	199.9	510.2
Slew Rate (GHZ)	**2.275**	0.0157	0.177	0.208	0.986
Write Static Noise Margin (WSNM) Volts	0.28	0.40	0.203	0.354	**0.55**

Table 3. Comparison of SRAM Cell for read operation using various approaches for input voltage 0.7 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Read Power Dissipation (µw)	2.327	0.889	1.229	**0.276**	**0.317**
Leakage Power dissipation during Read (pw)	15.9	24.486	9.36	14.076	**9.251**
Read Delay (ps)	**71.25**	264.3	264.2	202.9	**183.1**
Rise Time (ps)	7.73	4.628	**2.270**	4.692	4.735
Fall Time (ps)	10.44	**3.969**	7.54	16.91	19.96
Power Delay Product (aJ)	165.79	234.87	324.7	**56.0**	**58.04**
Settling Time (ns)	19.99	**15.19**	19.99	**15.19**	**15.19**
Slew Rate (GHZ)	0.02837	**9.683**	0.00519	9.50	**9.51**
Read Static Noise Margin (RSNM) Volts	0.178	0.27	0.054	**0.488**	**0.34**

Table 4. Comparison of SRAM Cell for write operation using various approaches for input voltage 0.7 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Write Power Dissipation (nw)	**3.959**	4.718	13.15	**4.048**	6.962
Leakage Power dissipation during Write (pw)	290.85	**9.206**	122.48	11.91	**9.33**
Write Delay (ps)	114.1	**39.84**	99.27	169.6	197.5
Rise Time (ps)	42.4	**4.30**	47.23	24.7	98.9
Fall Time (ps)	31.7	5.076	24.71	15.48	44.53
Power Delay Product (aJ)	0.451	**0.188**	1.305	0.686	1.374

Settling Time (ps)	162.3	**151.9**	191.2	199.9	255.9
Slew Rate (GHZ)	**6.796**	0.366	0.00955	0.00376	**2.923**
Write Static Noise Margin (WSNM) Volts	0.314	0.48	0.304	0.390	**0.605**

Table 5. Comparison of SRAM Cell for read operation using various approaches for input voltage 0.8 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Read Power Dissipation (µw)	5.581	1.76	2.917	**0.395**	**0.479**
Leakage Power dissipation during Read (pw)	23.149	39.85	12.37	18.117	**11.891**
Read Delay (ps)	**52.41**	263.4	263.7	99.15	105.4
Rise Time (ps)	6.97	3.063	**1.42**	2.894	2.913
Fall Time (ps)	3.56	**0.724**	6.96	7.837	8.677
Power Delay Product (aJ)	292.5	463.58	769.2	**39.16**	**50.48**
Settling Time (ns)	19.99	**15.2**	19.99	**1.52**	**15.2**
Slew Rate (GHZ)	0.026	**12.13**	0.0127	**11.96**	**11.77**
Read Static Noise Margin (RSNM) Volts	0.20	0.31	0.060	**0.488**	**0.38**

Table 6. Comparison of SRAM Cell for write operation using various approaches for input voltage 0.8 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Write Power Dissipation (nw)	**3.959**	4.718	13.15	**4.048**	6.962
Leakage Power dissipation during Write (pw)	290.85	**9.206**	122.48	11.91	**9.33**
Write Delay (ps)	114.1	**39.84**	99.27	169.6	197.5
Rise Time (ps)	42.4	**4.30**	47.23	24.7	98.9
Fall Time (ps)	31.7	5.076	24.71	15.48	44.53
Power Delay Product (aJ)	0.451	**0.188**	1.305	0.686	1.374
Settling Time (ps)	162.3	**151.9**	191.2	199.9	255.9
Slew Rate (GHZ)	**6.796**	0.366	0.00955	0.00376	**2.923**
Write Static Noise Margin (WSNM) Volts	0.314	0.48	0.304	0.390	**0.605**

Table 7. Comparison of SRAM Cell for read operation using various approaches for input voltage 0.9 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Read Power Dissipation (µw)	10.34	2.50	5.313	**0.528**	**0.671**
Leakage Power dissipation during Read (pw)	33.49	65.38	11.15	24.0	**14.942**

Read Delay (ps)	**44.33**	262.8	263.3	73.45	79.31
Rise Time (ps)	2.578	1.756	**0.931**	1.739	1.807
Fall Time (ps)	0.389	**0.232**	1.99	3.541	6.624
Power Delay Product (aJ)	458.3	657.5	1398.9	**38.78**	**53.21**
Settling Time (ns)	19.99	**15.2**	19.99	**15.2**	**15.2**
Slew Rate (GHZ)	0.284	**13.82**	2.018	**13.7**	**13.41**
Read Static Noise Margin (RSNM) Volts	0.212	0.350	0.062	**0.512**	**0.41**

Table 8. Comparison of SRAM Cell for write operation using various approaches for input voltage 0.9 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Write Power Dissipation (nw)	8.244	**6.724**	36.6	8.223	13.65
Leakage Power dissipation during Write (pw)	1986.2	25.28	347.068	19.61	**19.44**
Write Delay (ps)	**57.51**	69.24	99.73	103.1	97.58
Rise Time (ps)	23.51	**8.169**	94.29	110.4	45.95
Fall Time (ps)	24.47	5.083	17.19	3.512	30.2
Power Delay Product (aJ)	0.474	**0.465**	3.65	0.847	1.33
Settling Time (ps)	**108.0**	152.0	185.9	199.9	150.6
Slew Rate (GHZ)	**15.96**	0.454	0.0115	0.0591	**8.24**
Write Static Noise Margin (WSNM) Volts	0.354	0.620	0.378	0.478	**0.696**

Table 9. Comparison of SRAM Cell for read operation using various approaches for input voltage 1 V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Read Power Dissipation (µw)	16.34	3.32	8.424	**0.68**	**0.872**
Leakage Power dissipation during Read (pw)	47.072	107.42	19.81	27.91	**18.38**
Read Delay (ps)	**38.28**	262.2	262.9	58.98	68.52
Rise Time (ps)	1.766	0.972	**0.0465**	0.925	0.842
Fall Time (ps)	0.40	0.0918	**0.0079**	2.499	2.491
Power Delay Product (aJ)	625.4	870.5	2214.6	**40.10**	**59.74**
Settling Time (ns)	19.99	**15.2**	19.99	**15.2**	**15.2**
Slew Rate (GHZ)	0.0495	**15.02**	0.0020	14.46	**15.23**
Read Static Noise Margin RSNM (Volts)	0.22	0.40	0.65	**0.54**	**0.45**

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Table 10. Comparison of SRAM Cell for write operation using various approaches for input voltage 1V

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip LECTOR
Write Power Dissipation (nw)	12.39	**7.933**	58.96	12.19	19.15
Leakage Power dissipation during Write (pw)	4627.55	35.145	538.0	25.82	**22.374**
Write Delay (ps)	**48.89**	95.4	99.79	107.8	**78.77**
Rise Time (ps)	22.18	**11.25**	85.38	55.1	41.42
Fall Time (ps)	21.85	5.08	17.00	2.93	28.74
Power Delay Product (aJ)	**0.605**	0.757	5.88	1.314	1.508
Settling Time (ps)	**94.02**	152.0	184.3	200.0	131.5
Slew Rate (GHZ)	**18.8**	0.502	0.0164	0.058	**10.16**
Write Static Noise Margin (WSNM) Volts	0.375	0.70	0.403	0.502	**0.720**

$$P_{total} = P_{dynamic} + P_{short} + P_{static} \quad (1)$$

Where, $P_{dynamic}$ is the dynamic power dissipation which can be calculated by the equation (2)

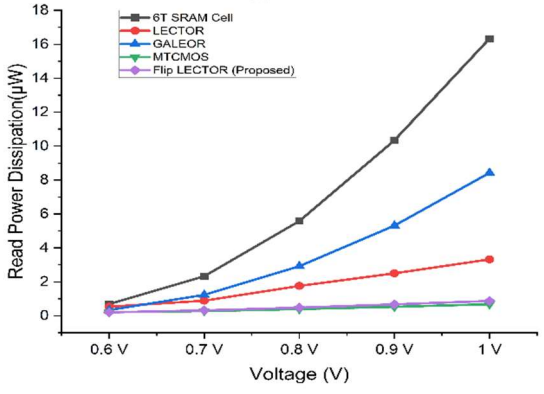
$$P_{dynamic} = 0.5 * V_{dd}^2 * f \quad (2)$$

Where P_{short} is the short circuit power which can be calculate by the equation (3)

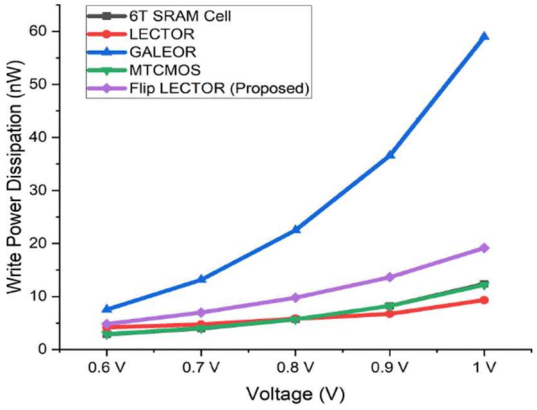
$$P_{\{short\ circuit\}} = I_{sc} * V_{dd} * f \quad (3)$$

Where Isc= short-circuit current when switching operation perform in the circuit, V_{dd}= supply voltage and f= switching frequency. P_{static} is the static power which can be calculate by the equation (4)

$$P_{static} = \left(I_{sub} + I_{gate} + I_{junct} + I_{contention}\right) * V_{dd} \quad (4)$$



(a)



(b)

Figure 7: Power Dissipation of SRAM cell using hybrid approaches at various voltages (a) Read, (b) Write

5.2 Leakage Power Dissipation

Due to varying input supplies, certain transistors in an SRAM cell are "ON" while others are "OFF" during read and write operations. Transistors drain energy while they are "ON," but they also lose energy when they are "OFF" [27]. The overall power dissipation of these "OFF" transistors is called run-time leakage power dissipation. When the supply voltage drops, the leakage power dissipation falls. Leakage current can be calculate by the equation 5.

$$I_{leak} = I_{off} * 10^{\left[\frac{\{V_{GS}+\eta(V_{ds}-V_{dd})-K_\gamma * V_{SB}\}}{S}\right]} \quad (5)$$

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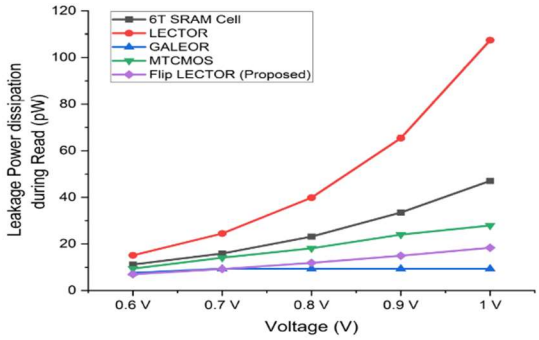
Where $I_{leakage}$= Leakage current, V_{dd}= supply voltage, I_{off}= subthreshold current, η = DIBL Coefficient, V_{SB}= source to body voltage and K_γ= Body effect coefficient

Total Leakage power can be calculate by the equation (6)

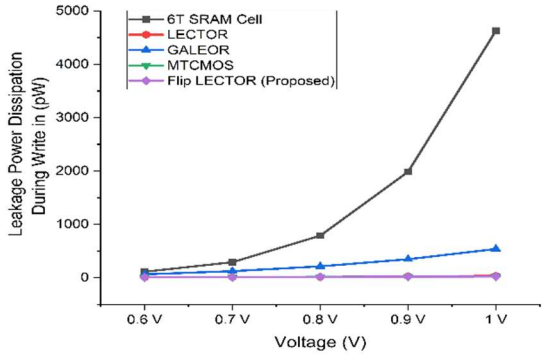
$$P_{Leakage} = I_{leakage} * V_{dd} \qquad (6)$$

Where $I_{leakage}$= Leakage current and V_{dd}= supply voltage

The proposed Flip LECTOR approach leakage power dissipation during read is 2.55×, 5.84×, 1.08× and 1.52× less as compared to conventional 6T SRAM cell, LECTOR, GALEOR and MTCMOS approach for 1V. A graphical representation of leakage power dissipation of read is shown in Fig. 8 (a). The proposed Flip LECTOR approach leakage power dissipation during write is 206×, 1.57×, 24×, and 1.15× less than in the conventional 6T SRAM cell, LECTOR, GALEOR, and MTCMOS approach for 1V. Fig. 8 (b) shows a graphical representation of leakage power dissipation during write. When Q = 1 and QB = 0, in this case PM3 transistor operates in cutoff region, and when Q=0 and QB= 1, in this case PM2 transistor operates in cutoff region so the leakage current reduced, hence leakage power dissipation reduced.



(a)



(b)

Figure 8: Leakage Power Dissipation during operation of SRAM cell using hybrid approaches at various voltages (a) Read, (b) Write

5.3 Read Delay and Write Delay

The read-and-write delay can be estimated when the word line is high. The time it takes to convey data from "Q" to BL or BLB is called "read delay". When the supply voltage increases, the circuit's delay diminishes exponentially [28]. When the supply voltage is raised, the read delay drops.

$$tpd = \frac{t_{plh} + t_{phl}}{2} \qquad (7)$$

The propagation delay is represented by the delay, which is defined as the average of the low-to-high progress delay (t_{plh}) and the high-to-low change delay (t_{phl}). This is expressed as, where t_{plh} and t_{phl} are taken from the generated waveforms of reading and writing operations (7). So, tphl is set when the input voltage changes from high to low and the output voltage changes from low to high. Similarly, tplh is set when the input voltage changes from low to high and the output voltage changes from high to low [15]. Flip LECTOR approach read delay is 3.82× and 3.83× lesser as compared to LECTOR and GALEOR approaches, respectively, consecutively 1.79× and 1.16× larger as compared to 6T SRAM Cell and MTCMOS approach, respectively. A graphical representation of the read delay is shown in Fig. 9 (a). The time it takes to transmit data from the BL or BLB to "Q" is known as the "write delay." When the supply voltage increases, the write delay likewise falls exponentially [29]. The flip LECTOR approach write delay for 1V is 1.21×, 1.26×, and 1.37× lesser than the LECTOR, GALEOR, and MTCMOS approaches, respectively, 1.61× larger than the 6T SRAM Cell. A graphic representation of the write delay is shown in Fig 9 (b).

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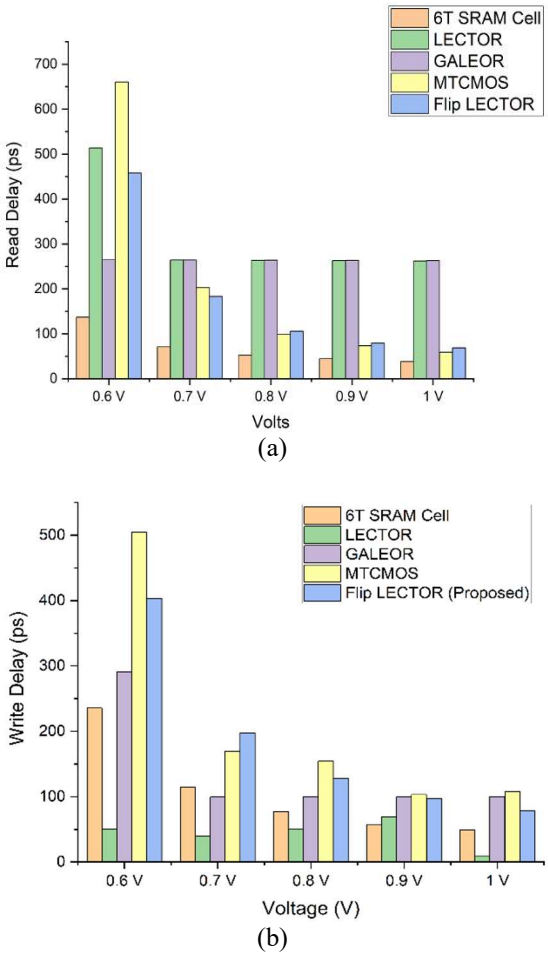


Figure 9: Delay of SRAM cell using hybrid approaches at various voltages (a) Read, (b) Write

5.4 Rise Time and Fall Time

The time required for a pulse to increase from 10% to 90% of its steady state value is known as the rise time. When the supply voltage is raised, the circuit's rise time is reduced [30]. Flip LECTOR approach rise time for a read operation is 2.09×, 1.154×, and 1.098× less as compared to 6T SRAM Cell, LECTOR, and MTCMOS approach and 18.75× larger as compared to the GALEOR approach. A graphical representation of the rise time for a read operation is shown in Fig.10 (a). The time it takes for a pulse to decline from 90% to 10% of its steady state value is known as "fall time." When the supply voltage increases, the circuit's fall time also falls [31]. Flip LECTOR Approach fall time for read operation is 6.23×, 27.15×, and 315× larger than the Traditional 6T SRAM Cell, LECTOR, and GALEOR approach and 1.0032× smaller than the MTCMOS approach. A graphic representation of fall time for read operation is shown in Fig. 10 (b).

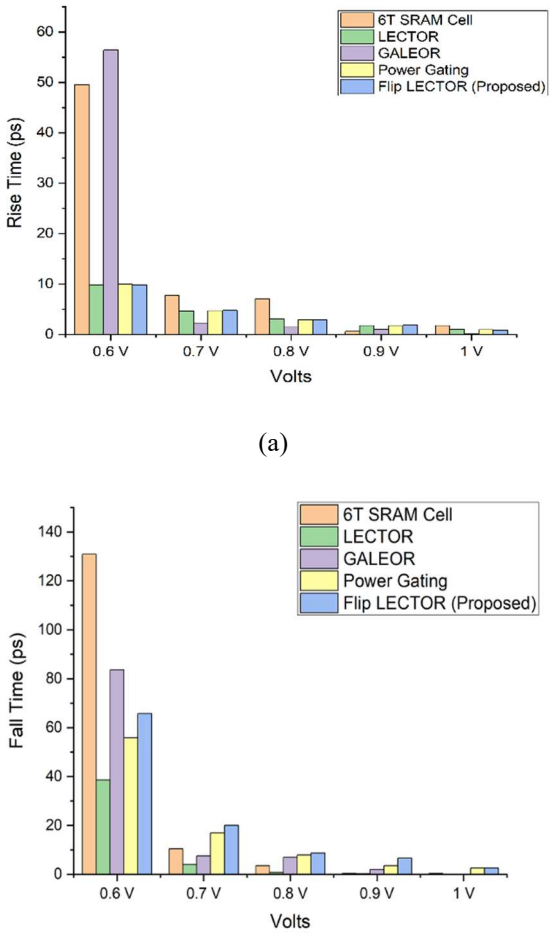
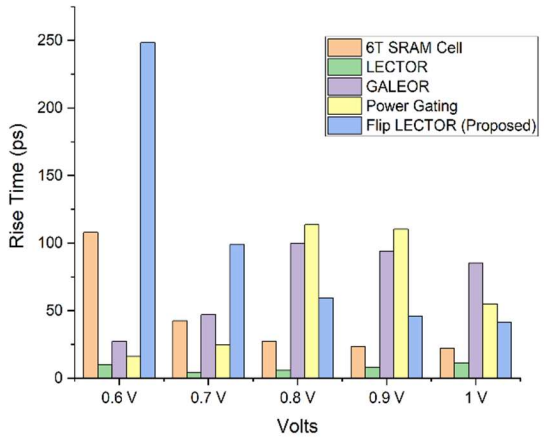
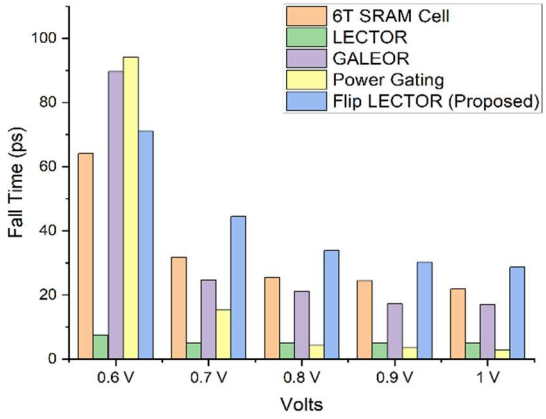


Figure 10: Read operation for SRAM cell using hybrid approaches at various voltages (a) Rise Time, (b) Fall Time

The flip LECTOR approach rise time of write is 1.867×, 3.68× larger than that of a 6T SRAM cell, LECTOR approach, and 2.061×, 1.33× lesser than that of a GALEOR and MTCMOS approach. A graphic representation of the rise time for the write operation is shown in Fig.11 (a). When the supply voltage rises, the fall time of the write operation for the SRAM cell also lowers [33]. The proposed Flip LECTOR approach is 1.31×, 5.65×, 1.69×, and 9.8× larger than the Traditional 6T SRAM Cell, LECTOR, GALEOR, and MTCMOS approach. Fig. 11 (b) shows a graphic representation of the fall time for the write operation.



(a)

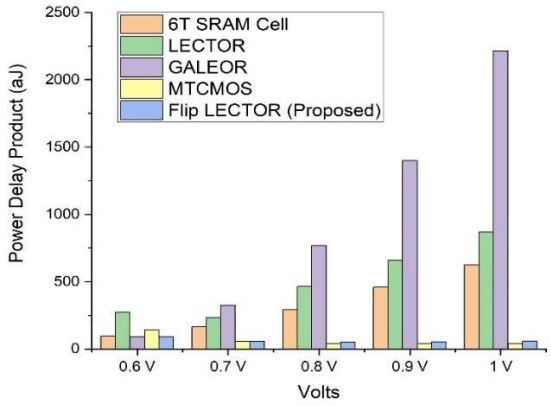


(b)

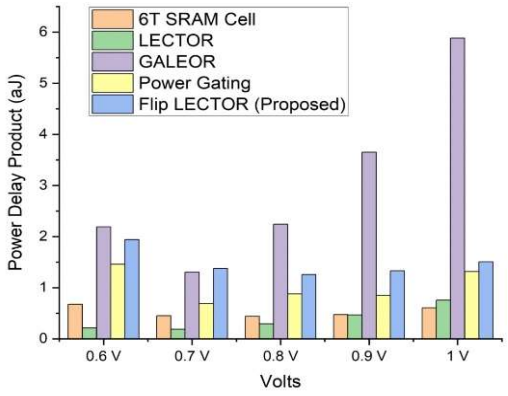
Figure 11: Write operation for SRAM cell using hybrid approaches at various voltages (a) Rise time, (b) Fall Time

5.5 Power Delay Product

The power delay product, a measurement of the switching efficiency of digital logic-based circuits, is one such parameter. Total power dissipation and measurement delay are multiplied to compute it [34], shown in Fig. 12(a). The power delay product of the proposed Flip LECTOR method for the read operation is 10.46×, 14.57×, and 37.07× larger as compared to the 6T SRAM cell, LECTOR, and GALEOR approach, respectively, and 1.489× lesser as compared to MTCMOS approach. The power delay product of the proposed Flip LECTOR method for the write operation is 2.49×, 1.99×, and 1.15× larger than those of the 6T SRAM cell, LECTOR, and MTC MOS approaches, respectively, and 3.90× smaller than those of the GALEOR approach. A graphic representation is shown in Fig. 12(b).



(a)



(b)

Figure12: Power delay product of operation for SRAM cell using hybrid approaches at various voltages for (a) Read, (b) Write

5.6 Settling Time

Settling time is the amount required for an output to reach its final value after propagation delay has been included, as shown in Figs. 13(a). When the supply voltage rises, the settling time reduces or remains constant [35-36]. The proposed Flip LECTOR method of read operation settling time is 1.32× smaller than the 6T SRAM cell and GALEOR approach. The setting time of the write operation is 1.40× and 1.15× larger compared to the 6T SRAM cell and LECTOR approaches, respectively, 1.40×, 1.52× lesser compared to the GALEOR and MTCMOS approaches. A graphic representation is shown in Fig. 13(b).

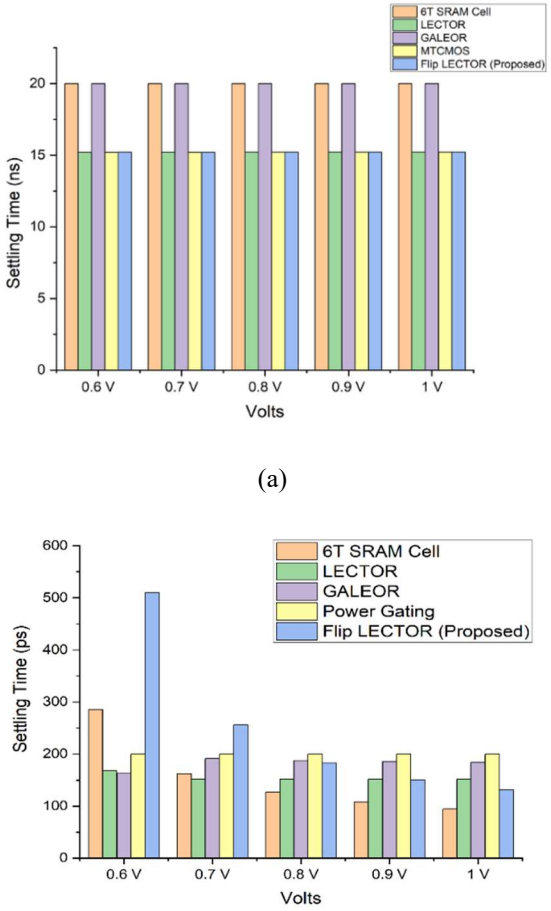


Figure 13: Settling time of operation for SRAM cell using hybrid approaches at various voltages of (a) Read, (b) Write

5.7 Slew Rate

The highest output amplitude generated about time is called the slew rate. The slew rate in terms of frequency is the inverse of time. If the output voltage becomes constant, then the slew rate in terms of frequency may be computed. The proposed Flip LECTOR approach read operation has a slew rate for 1V that is 307×, 1.01×, 7615×, and 14.46× larger than that of the Traditional 6T SRAM Cell, LECTOR, GALEOR, and MTCMOS approach. A graphic representation is shown in Fig.14 (a). The proposed Flip LECTOR approach write operation has a slew rate for 1V that is 20.23×, 619.5×, and 175.17× larger, respectively, than the LECTOR, GALEOR, and MTCMOS approaches and 1.85× smaller than the 6T SRAM cell. A graphic representation is shown in Fig. 14 (b).

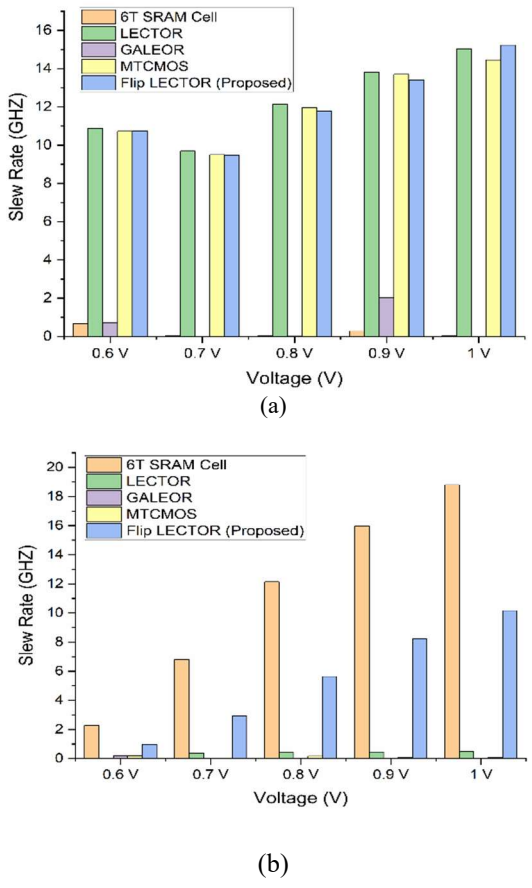
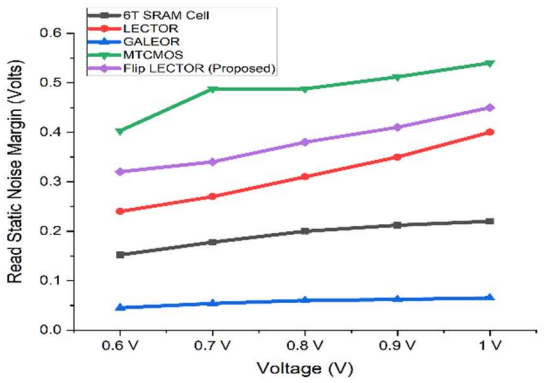


Figure 14: Slew rate of operation for SRAM cell using hybrid approaches at various voltage of (a) Read, (b) Write

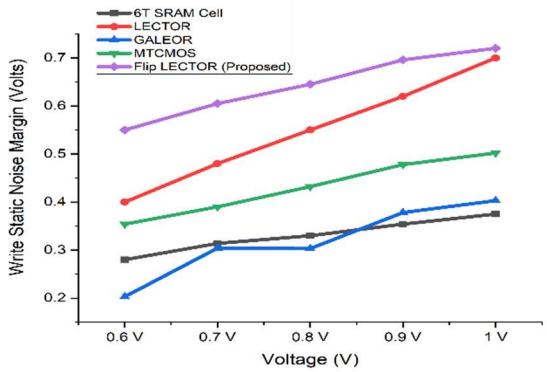
5.8 Read Static Noise Margin and Write Static Noise Margin

When determining stability in memory design, static noise margin is the most crucial factor. Construct the butterfly curves for the SRAM cell before computing the static noise margin, then fit the most considerable square size into the butterfly structure. This square or rectangle touches the butterfly structure boundaries [39]. The horizontal length of the square or rectangle provides the value of the static noise margin. This static noise margin is referred to as WSNM for writes and RSNM for reads in the context of a given operation [42], as shown in Fig. 15(a) and (b). The proposed Flip LECTOR approach RSNM is 2.04× and 1.12× larger as compared to the 6TSRAM cell and LECTOR approach, respectively, 6.92× and 1.20× lesser as compared to the GALEOR and MTCMOS approach. The proposed Flip LECTOR approach WSNM is 1.92×, 1.03×, 1.78× and 1.43× larger as compared to the 6T SRAM cell, LECTOR,

GALEOR, and MTCMOS approach.



(a)



(b)

Figure 15. Static noise margin of SRAM cell using hybrid approaches at various voltages for (a) Read, (b) Write

5.9 Layout Area Estimation

The proposed approach's layout area has been compared with the traditional 6T SRAM, LECTOR, GALEOR, and MTCMOS approaches. The layouts have been drawn using a Micro-wind tool with a 65nm technology node Table 11 lists the number of transistors used and compares them with the area of a traditional 6T SRAM cell. The 6T SRAM cell contains the lowest layout among all the SRAM cell-based leakage reduction approaches. The proposed approach occupies a larger area 1.95×, 1.07×, 1.47×, and 1.57× as compared to the traditional 6T SRAM, LECTOR, GALEOR, and MTCMOS approaches. In the proposed Flip LECTOR approach, 10 transistors are used, but the area is increased due to wiring and connections. The proposed approach overcomes this demerit by the various merits of stability, low leakage power, read power, and quality signal, as with other approaches used in this paper.

Table 11. Area comparison of SRAM Cell using various approaches

Various Approaches	6T SRAM Cell	LECTOR	GALEOR	MTCMOS	Proposed Flip-LECTOR
Area (μm^2)	1×	1.80×	1.32×	1.24×	1.95×
Transistors Count	6	10	10	8	10

6. SUMMARY OF 6T SRAM CELL AND LEAKAGE POWER REDUCTION APPROACHES

Table 12. Summary of 6T SRAM Cell and Leakage power reduction approaches

Various Approaches	Advantages	Disadvantages
6T SRAM Cell	This cell is easy to design because it design without leakage power reduction approaches. Less number of transistors are required.	This cell leakage power dissipation is high.
LECTOR	This cell leakage power saving is better, also to monitor leakage additional circuit is not required	Its signal quality is not good.
GALEOR	This cell leakage power saving is better, also to monitor leakage additional circuit is not required	Its signal quality is poor than LECTOR approach
MTCMOS	It is a industry preferred approach, because of high leakage power saving	Delay penalty, due to additional mask layers, the fabrication process becomes complex, Also data retention problem controller design is required
Proposed Flip-LECTOR	This approach have all advantage as of basic 6T SRAM cell, also its leakage power saving is very high in read and write operation both. Its signal quality is also high.	Area is higher than LECTOR and GALEOR approaches

7. CONCLUSION

In this research paper, the Proposed approach exhibits favorable performance in the voltage range of 0.6V to 1V concerning read power dissipation, leakage power during read and write operations, power delay product, settling time, slew rate, and read and write stability. The read power, write power, stability, access time, power delay product, slew rate, settling time and leakage power dissipation are calculated and analyzed using CADENCE Virtuoso tool in 45nm technology node. Also all the circuits are simulated with suitable cell ratio and pull up ratio. In detail Flip LECTOR based 6T SRAM cell leakage power dissipation during read and write operations is reduced by 2.55×, 5.84×, 1.08×, 1.52×, and 206×, 1.57×, 24×, 1.15× compared to traditional 6T SRAM cells, LECTOR, GALEOR, and MTCMOS approaches for 1V. In proposed approach read power is reduced by 18.73×, 3.8×, and 9.67× as of conventional 6T SRAM cell, LECTOR, and GALEOR approaches and increased by 1.28× as of the MTCMOS approach for 1V. The read settling time is reduced by 1.32× as of the 6T SRAM cell and GALEOR approach, and the write settling time is also reduced by 1.40× as of the 6T SRAM cell and LECTOR approach. The proposed approach has trade-off in terms of area due to its number of transistors and its design.

REFERENCES:

[1] V.K. Sharma. "A survey of leakage reduction techniques in CMOS digital circuits for nanoscale regime." *Australian journal of electrical and electronics Engineering* 18.4, 217-236, 2021. DOI: https://doi.org/10.1080/1448837X.2021.1966957.

[2] K. Gavaskar, U. S. Ragupathy, and V. Malini, "Design of novel SRAM cell using hybrid VLSI techniques for low leakage and high speed in embedded memories," *Wireless Personal Communications* 108(4), 2311-2339, 2019. DOI: https://doi.org/10.1007/s11277-019-06523-7.

[3] R. Lorenzo and S. Chaudhury, "Review of circuit level leakage minimization techniques in CMOS VLSI circuits," *IETE Technical review*, 34(2), 165-187, 2017. DOI: https://doi.org/10.1080/02564602.2016.1162116.

[4] V.K. Sharma and M. Pattanaik, "Techniques for low leakage nanoscale VLSI circuits: A comparative study," *Journal of Circuits, Systems, and Computers*, 23(5), 1450061, 2014. DOI: https://doi.org/10.1142/S0218126614500613

[5] R. Lorenzo and S. Chaudhury, "A novel SRAM cell design with a body-bias controller circuit for low leakage, high speed and improved stability,"

Wireless Personal Communications, 94(4), 3513-3529, 2017. DOI: https://doi.org/10.1007/s11277-016-3788-5.

[6] K.K. Kim, Y.B. Kim, M. Choi, and N. Park, "Leakage minimization technique for nanoscale CMOS VLSI," *IEEE Design & Test of Computers*, 24(4) 322-330, 2007. DOI: https://doi.org/10.1109/MDT.2007.111.

[7] Abdollahi, F. Fallah, & M. Pedram, "Leakage current reduction in CMOS VLSI circuits by input vector control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* 12(2) 140-154, 2004. DOI: https://doi.org/10.1109/TVLSI.2003.821546.

[8] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, 91(2), 305-327, 2003. DOI: https://doi.org/10.1109/JPROC.2002.808156.

[9] R. Lorenzo and S. Chaudhury, "Dynamic threshold sleep transistor technique for high speed and low leakage in CMOS circuits," *Circuits, Systems, and Signal Processing*, 36(7), 2654-2671, 2017. DOI: https://doi.org/10.1007/s00034-016-0442-0.

[10] Neil HE Weste, and David Harris, "CMOS VLSI design: a circuits and systems perspective," *Pearson Education India*, 2015. DOI: https://doi/10.5555/1841628.

[11] R. Lorenzo and S. Chaudhury, "LCNT-an approach to minimize leakage power in CMOS integrated circuits," *Microsystem Technologies*, 23(9), 4245-4253, 2017. DOI: https://doi.org/10.1007/s00542-016-2996-y.

[12] A. Calimera, E. Macii, and M. Poncino, "Design techniques and architectures for low-leakage SRAMs," IEEE Transactions on Circuits and Systems I: Regular Papers, 59(9), 1992-2007, 2012. DOI: https://doi.org/10.1109/TCSI.2012.2185303.

[13] H. Kumar and V.K. Tomar, "A review on performance evaluation of different low power SRAM cells in nano-scale era," *Wireless Personal Communications*, 117(3), 1959-1984, 2021. DOI: https: //doi.org/10.1007/s11277-020-07953-4.

[14] S. Katrue, and D. Kudithipudi, "GALEOR: Leakage reduction for CMOS circuits," *15th IEEE International Conference on Electronics, Circuits and Systems*, pp. 574-577, 2008. DOI: https://doi.org/10.1109/ICECS.2008.4674918.

[15] Singh, Jawar, Saraju P. Mohanty, and Dhiraj K. Pradhan, "Robust SRAM designs and analysis," *Springer Science & Business Media,* 2012. DOI: https: //doi.org/10.1007/978-1-4614-0818-5.

[16] P. Corsonello, M. Lanuzza and S. Perri, "Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates," *International journal of circuit theory and applications*, 42(1), 65-70, 2014. DOI: https://doi.org/10.1002/cta.1838.

[17] N. Hanchate and N. Ranganathan, "LECTOR: a technique for leakage reduction in CMOS circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 12(2), 196-205, 2004. DOI: https://doi.org/ 10.1109/TVLSI.2003.821547.

[18] R. Yadav, & R. Yadav, "Dynamic Power Reduction Techniques for CMOS Logics Using 45 nm Technology," *International Conference on Intelligent Computing and Smart Communication springer*, pp. 1117-1126, 2019. DOI: https://doi.org/10.1007/978-981-15-0633-8_112.

[19] S. Chaudhury and R. Lorenzo, "Leakage Minimization in CMOS VLSI Circuits: A Brief Review," *Design and Modelling of Low Power VLSI Systems*, pp.71-99, 2016. DOI: https://doi.org/10.4018/978-1-5225-0190-9.CH004.

[20] Y.G. Chen, H. Geng, K.Y. Lai, Y. Shi and S.C. Chang, "Multibit retention registers for power gated designs: Concept, design, and deployment," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 33(4), 507-518, 2014. DOI:https://doi.org/10.1109/TCAD.2013.2293881.

[21] N. Tiwari, P. Atre, P. Parihar, and V. Neema, "Highly robust asymmetrical 9T SRAM with trimode MTCOS technique," *Microsystem Technologies*, 25(5), 1593-1598, 2019. DOI: https://doi.org/10.1007/s00542-017-3434-5.

[22] E.N. Shauly, "CMOS leakage and power reduction in transistors and circuits: process and layout considerations," *Journal of Low Power Electronics and Applications*, 2(1), 1-29, 2012. DOI: https://doi.org/10.3390/jlpea2010001.

[23] P. Saini and R. Mehra, "Leakage power reduction in CMOS VLSI circuits," *International Journal of Computer Applications,* 55(8), 2012. DOI: https://doi.org/10.5120/8778-2721.

[24] S.G. Narendra and A.P. Chandrakasan, "Leakage in nanometer CMOS technologies," *Springer Science & Business Media* 2006. DOI: https://doi.org/10.1007/0-387-28133-9.

[25] A. Bellaouar and M. Elmasry, "Low-power digital VLSI design: circuits and systems," *Springer Science & Business Media* 2012. DOI: https://doi.org/10.1007/978-1-4615-2355-0.

[26] N. Jayakumar, S. Paul, and R. Garg, "Minimizing and exploiting leakage in VLSI design," *Springer Science & Business Media* 2009. DOI: https://doi.org/10.1007/978-1-4419-0950-3.

[27] Friedman, G. Eby and Volkan Kursun, "Multi-voltage CMOS circuit design," 2006. DOI: *doi/book/10.1002/0470033371*.

[28] Sil, S. Ghosh, N. Gogineni and M. Bayoumi, "A novel high write speed, low power, read-SNM-free 6T SRAM cell," *51st Midwest Symposium on Circuits and Systems*, pp. 771-774, 2008. DOI: https://doi.org/10.1109/MWSCAS.2008.4616913.

[29] Pavlov, and M. Sachdev, "CMOS SRAM circuit design and parametric test in nano-scaled technologies: process-aware SRAM design and test" *Springer Science & Business Media* 2008. DOI: https://doi.org/10.1007/978-1-4020-8363-1.

[30] D. Anitha, K. Manjunathachari, P. Sathish Kumar and G. Prasad, "Design of low leakage process tolerant SRAM cell," *Analog Integrated Circuits and Signal Processing*, 93(3) 531-538, 2017. DOI: https://doi.org/10.1007/s10470-017-1061-9.

[31] M.A. Rahma, and M. Anis, "Nanometer variation-tolerant SRAM: circuits and statistical design for yield," Springer Science & Business Media 2012. DOI: https://doi.org/10.1007/978-1-4614-1749-1.

[32] J.K. Mishra, B.B. Upadhyay, P.K. Misra, and M. Goswami, "Design and analysis of SRAM cell using body bias controller for low power applications." *Circuits, Systems, and Signal Processing*, 40(5), 2135-2158, 2021. DOI: https://doi.org/10.1007/s00034-020-01578-5.

[33] V. Sharma, F. Catthoor, and W. Dehaene, "SRAM Design for Wireless Sensor Networks," *Analog circuits and signal processing*, pp.9-30, 2013. DOI: https://doi.org/10.1007/978-1-4614-4039-0.

[34] Sachdeva & V.K. Tomar, "Design of low power half select free 10T static random-access memory cell," *Journal of Circuits, Systems and Computers,* 30(04), 2150073, 2021. DOI: https://doi.org/10.1142/S0218126621500730.

[35] Kurinec, K. Santosh, and Krzysztof Iniewski, "Nanoscale semiconductor memories: technology and applications," CRC press, 2013. DOI: https://doi.org/10.1201/b16236.

[36] Sachdeva and V.K. Tomar, "Design of a stable low power 11-T static random access memory cell," *Journal of circuits, Systems and Computers*, 29(13), 2050206, 2020. DOI: https://doi.org/10.1142/S0218126620502060.

[37] Itoh, Kiyoo, Masashi Horiguchi, and Hitoshi Tanaka, "Ultra-low voltage nano-scale memories," Springer Science & Business Media, 2007. DOI: https://doi.org/10.1007/978-0-387-68853-4.

[38] G. Prasad, and A. Anand, "Statistical analysis of low-power SRAM cell structure," *Analog Integrated Circuits and Signal Processing,* 82(1), 349-358, 2015. DOI: https://doi.org/10.1007/s10470-014-0463-1.

[39] S. Dasgupta, "6T SRAM cell analysis for DRV and read stability," *Journal of Semiconductors,* 38(2), 025001, 2017. DOI: https://doi.org/10.1088/1674-4926/38/2/025