Journal of Theoretical and Applied Information Technology
30th April 2025. Vol.103. No.8

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

HYBRID TYPE ERROR CORRECTION CODE TO INCREASE RELIABILITY IN SRAM MEMORIES

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ABSTRACT

This paper presents implementation of mixed mode Error Correction Coder architecture that is capable of detecting and correcting both random and burst. The proposed architecture executes two different types of architectures in which one of them aims at targeting the random while the other aims at burst. The diagnosis of random faults is obtained by employing the modified decimal matrix coding whereas the burst diagnosis is done by flexible unequal error method. The proposed architecture gains an adequate advantage with respect to area overhead and power consumption. The proposed architecture is implemented in cadence. In the front end design the parameters are estimated by using out by GENUS and on similar lines, the back end design is carried out by using out by INNOVUS and the performance metric generated includes Area Report, Power Report, and timing report and chip layout. The area, power and delay overhead of the proposed architecture is found to be 50088.491, 20.7mW and 2.11ps which are very small compared to other ECC that are taken for experimental purpose and this low values of area, power and delay are mainly due to the use of encoder reuse technique. Further the experimental results conclude fact that the proposed architecture can achieve 100% of error correction up to six bits and offers correction rate of 80.76 and 68.43 for burst of length 7 and 8 respectively. The error correction capabilities for random error is found to be 100% for Quintuple Bit Error and there after we observed slight decrement in error correction capability for Sextuple Bit, Septuple bit and Octuple Bit. The percentage of error correction rate for Sextuple bit, Septuple bit and Octuple bit is found to be 46, 4 and 2 respectively. The increased reliability of this hybrid type error correction code is achieved at a cost of slight increment in the overhead bits.

Keywords: *Random errors, Burst errors, Modified Decimal Matrix code (MDMC), Flexible Unequal Error Control (FUEC), and Error Correction Code (ECC).*

1. INTRODUCTION

The proposed architecture is obtained by the integration of two different types of namely Modified Decimal Matrix Coder (MDMC) [39] and Enhanced Flexible Unequal Error Correction Code [40]. The Decimal Matrix Code offers a very high correction rate for diagnosing random errors. The high correction rate in DMC is achieved at the cost of increased area over head and power consumption. However based on our experimental study few modifications were suggested in the architecture of Decimal Matrix Coder (DMC) to yield improvements with respect to area overhead and power consumption without disturbing the inhertent property of DMC to achieve high correction rate. Thus MDMC aims at targeting random that occurs in memories for achieving very high correction rate with reduced power consumption and area overhead.

The other technique namely, Flexible Unequal Error Correction Code is very effective in handling the burst and achieving almost 100% error correction rate up to 4 bits. Flexible Unequal Error Correction Code is further enhanced to increase 100% burst error correction rate up to 5 bits and further, this Enhanced Unequal Error Correction Code achieves 100% error correction rate for burst error of length

6bit and as well as 7 bit depending on the probability of random being a part of burst length. All the previous studies address the issues like targeting single and double adjacent error detection and correction, neglecting random with increased power consumption and increased area over head. Here we present a novel architecture that employs encoder reuse technique that significantly reduces hard ware overhead by yielding reduction in power consumption as by product. The proposed architecture aims at detecting random as well as adjacent upto 6 bits that drastically increases error correction rate of the proposed method.

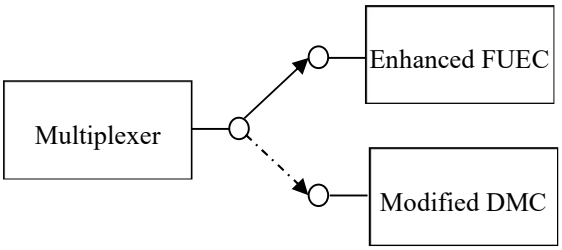

Fig 1. Basic Principle of Proposed ECC

The basic principle involved in the working proposed architecture is shown in fig.1. The diagnosing of memory is carried under two phases. The first phase of testing is carried out by Modified DMC to target random. Basic experimental studies convey fact that random can be easily detected by employing random test patterns and hence they are also termed as easy to detect or soft. The other phase of testing is carried out by Enhanced Flexible Unequal Error Correction Code (EFUEC) to detect burst errors. The burst error refers to presence of error in contiguous bits and these are effectively handled by Enhanced FUEC. Thus the proposed architecture is successful in diagnosing both random as well as burst.

Further, for better understanding of proposed mechanism, the paper is organized under following sections. Related technical development is presented in section II. The detailed architecture of the proposed method is provided in section III. Results drawn from the proposed architecture is given in section IV. Conclusion along with the future scope is presented in section V.

2. RELATED WORK

The initial seed for error correction using ECC's is laid by Richard W. Hamming [1] by introducing Hamming code. In general hamming codes allow only a single bit error correction, however a modified hamming [2-4] codes able to detect short burst. Hamming code using replication [5] effective against handling triple soft in memories. Hamming codes along with redundancy techniques [6] can effectively handle soft errors in memories that are employed for space applications. A new CLC algorithm [7] using extended hamming code can detect and correct multiple errors is memories that are employed for space applications. The CLC methodology is best fit for single bit and double bit error values, and reasonably significant for triple bit error values with inferior performance. This methodology is not fit for higher bit error values and specifically it is not addressed the adjacent error values.

Reed Muller [8] codes are being effectively employed in wireless communication more particularly in deep space communications and optical communications [9]. Symmetric Reed Muller codes [10-12] are effective in correcting locally. Berger codes [13] is successful in detecting all unidirectional that have been flipped from zero's one's or one's to zero's. These codes find its application in the design of BIST technologies [14] for combinational circuitry and ROM memories more particularly in DRAMs [15, 16] and CAM's [17] for detecting, correcting, and localizing unidirectional. Reed- Solomon code [18] are popularly employed for correcting burst in mass storage find its application in Satellite Communications and image processing techniques for space applications. A method of automatic polynomial selection for RS codes has been given in [19] to improve fault tolerance in embedded memories

Cyclic Redundancy Check [20] is popularly employed for detecting error in telecommunication networks and storage devices. This can also correct of double bit [21] and single burst error [22] effectively. Further it can be effectively employed for error detection in high speed semiconductor memories [23, 24]. Single Device Data Correction decoding scheme [25] can achieve 100% error detection rate for DRAM.

The mix codes or hybrid codes that combine one or more error detecting codes are successfully employed for protecting the memories from the cell upsets. The combination of LDPC and hamming code [26], BCH and LDPC [27] and LDPC with majority logic along with difference set codes [28] were quite successful in protecting the memories from cell upsets to a great extent. Another class of mix code combining error correction capabilities DMC and PMC codes has been designed [29] to detect multiple cell upsets that can yield

better performance with respect to maximum error correction with complete error detection.

In modern architectures, the memories are generally protected with SEC codes due to their simplicity in architecture. Pedro Reviriego et, al [30, 31] difference set codes can successfully correct triple bit with reasonable hardware requirements. The [32, 33] presents a matrix The existing methods discussed in the relevant work did not focused on addressing the adjacent. Addressed only the random. DMC and M-DMC methods proved as reliable methods to address random. But the power dissipation with respect to the leakage power, internal power, switching power and total power is not addressed for higher bit error rate values. The proposed method is focused to minimize the area with improved performance, to minimize the total dissipating power by minimizing the internal power, switching power, and leakage power, to detect and correct the random and adjacent and addressing the higher bit error values with minimum redundant bits.

3. PROPOSED ARCHITECTURE

The proposed architecture of fault diagnosis mechanism is composed of two architectures namely Modified Decimal Matrix Coder and Enhanced Flexible Unequal Error Correction Coder. The Modified Decimal Coder [39] is employed to target soft, whereas Enhanced Flexible Unequal Error Correction Coder [40] is employed to target burst. The detailed description of both the Error Correction Codes is presented as follows.

3.1 Enhanced Flexible Unequal Error Control (FUEC):

The general structure of Enhanced Flexible Error Correction Coder is given in fig.2. The raw data is fed into the data partitioning module which partitions data into different segments after which it is fed into the code rate allocation. The code rate allocation modules a segment assigned by the priority assignment block and coding mechanism that makes use of hamming and parity codes to assure reliability. These codes were also successful in detecting adjacent error's [34]. Improved Redundant matrix code [35] is also successfully employed to detect and correct cell upsets is SRAM's. Further, a much significant step in protecting the memories is laid by Decimal Matrix [36, 37 and 38]. M-DMC and DMC methods.

The process of encoding in its simple form is well explained in fig.3. The figure shows four steps. The step 1 includes original data which is represented with green color here, we assumed all bits to be 0's.The second step shows error injection, here an 8 bit error is injected and this forms burst error of 8 bit length i.e., 50% of data is corrupted and corrupted data is indicated with red color. The step 3 shows process of generating the syndrome

Final the encodes the data depending on the type of error correction code that has to be applied. Here same error correction code or different error correction codes for different segments can be chosen depending on the intended correction rates. Finally the stream combiner combines entire encoded data with different correction rates into a single data stream and makes it ready for storage or transmission.

The working of Enhanced Flexible Error Control Encoder is similar to working of any other error control encoder. However, this is mainly designed to provide different levels of error protection for different parts of the data by selecting different error correction codes for different segments of data. For better understanding of Enhanced FUEC and simplifying the complexities in the design of proposed mixed mode error correction code we limit the application of hamming code , parity code and redundancy check mechanisms for protecting the data. The critical data is encoded by generating the code word by the use of hamming code, parity code and redundancy check mechanisms. The remaining data is encoded with use of either hamming code or parity code or else with redundancy check mechanism depending on the significance of the data that has to be protected. The advantage of using same encoders in

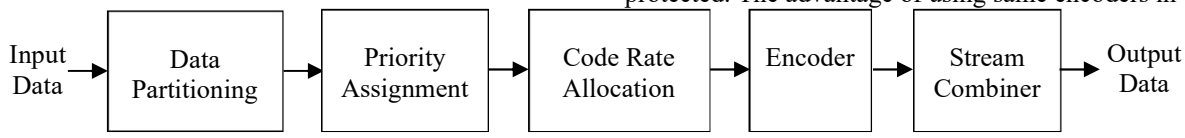

Fig.2 Block diagram of enhanced flexible Unequal error control coder

Modified Decimal Matrix Coding and Enhanced Flexible Error Control Coding aids in minimizing

error detection capability as well as the encoder-reuse technique (ERT) to minimize the area overhead of extra circuits (encoder and decoder) without disturbing the whole encoding and decoding processes, because ERT uses proposed encoder is itself to be part of the decoder.

that is obtained by performing XOR operation with original data and erroneous data. Finally step 4 illustrates the process extracting the error locations in original data with the aid of hamming matrix and the syndrome. The erroneous data present in the error locations is corrected by inverting the respect bits. The different formulae in [40] using Syndrome and code bits are employed in generating H-Matrix.

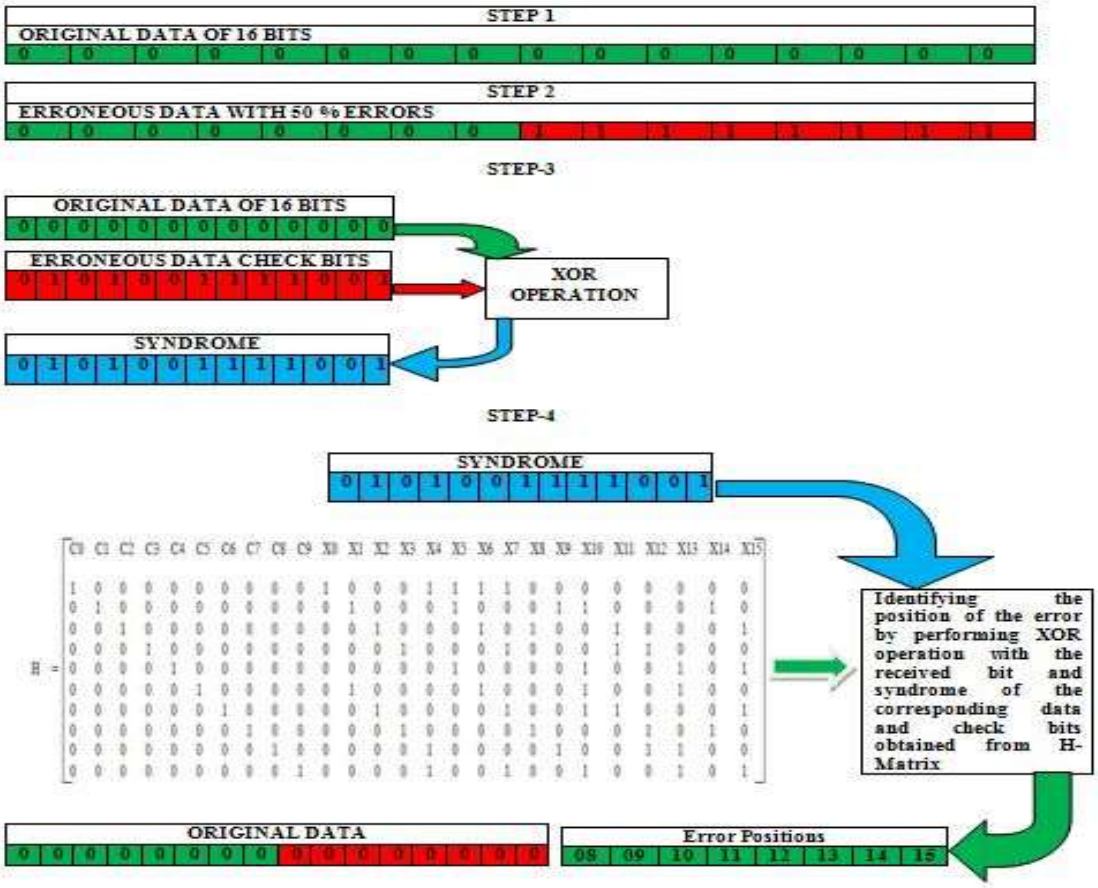

Fig.3 *Encoding Process in proposed mixed code encoder*

The block diagram of Enhanced Flexible Unequal Error Control System (EFUEC) is given in fig.4. The block diagram incorporates encoder, Syndrome generator, Error Detection Unit and decoding unit along with the memory used for storing encoded data and redundant bits. The encoder receives data that has to be protected from through data in and then the encoder adds check bits to the data ensuring that different that can be occurred over the data can be detected and corrected. The encoded data along with their corresponding check bits are stored in the memory. The encoded data available in memory is then given to the syndrome generator. The syndrome is computed by comparing the received data against error correcting code rules. The zero value of syndrome ensures that the data is error free and if the Syndrome is non-zero then the data is assumed to be erroneous. The erroneous data is then fed to the look up table for further processing. In look up table the syndrome value is compared against pre-computed error patterns in the look up table to provide information regarding the type of error and their positions. The decoder is employed to detect and correct the bits that are present in the received encoded data. The decoder receives encoded data along with the type and position of the error from

look up table and thus it inverts the value of the bits present in error locations yielding correct data. A few general control signals are also presented for ensuring its proper operation. The clock signal is used to synchronize the different operations associated with system. The enable is used to enable encoding and decoding operations and reset pin is used reset a system for a fresh start.

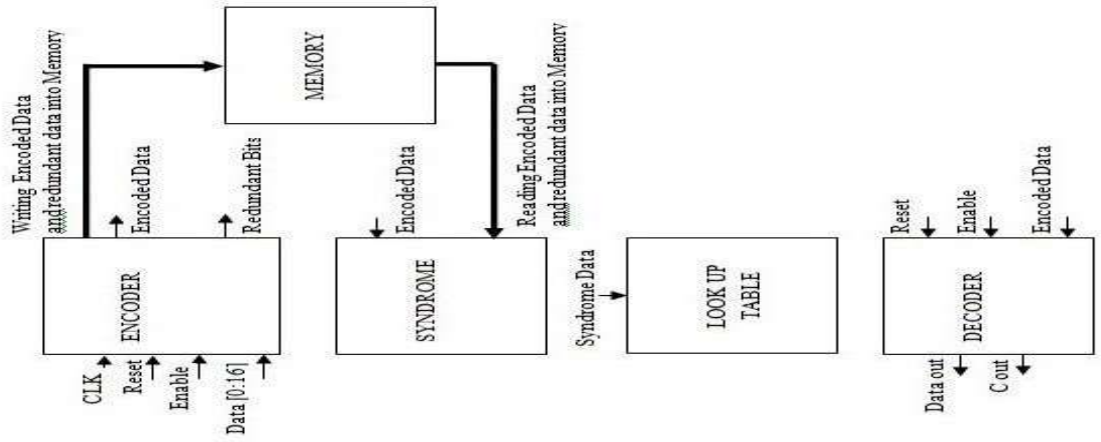

Fig.4. Enhanced Flexible Unequal Error Control System

3.2 Modified Decimal Matrix Code (MDMC) ENCODER

The modified DMC encoder employs hamming code for calculated overhead data bits. The circuit employed for formulating check bits composes of hamming encoder and XOR gates is shown in fig.5. The 'N' bit data taken from source is divided into 'k' symbols, each symbol is of m-bit length that yields N=k×m and these symbols are arranged analytically in a k1×k2 matrix form such that k=k1×k2, where k1 indicates rows and k2 indicates columns. The horizontal check bits are formulated by using hamming codes for each symbol of first row and thus each symbol is measured as decimal integer. The vertical check bits are formulated by using XOR operation for every column.

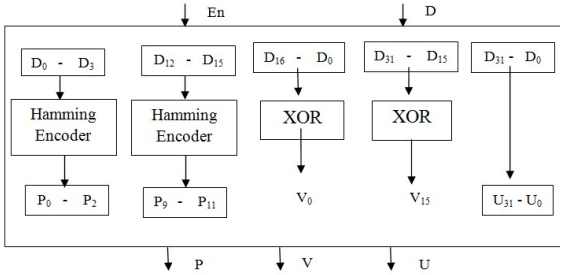

Fig. 5. Architecture of Modified DMC Encoder

Modified Decimal Matrix Code (MDMC) Decoder

The decoder shown in fig.6. is used to detect and correct the consequently. The received data bits 'D' are applied to the inbuilt encoder block in the decoder block to obtain horizontal check bits 'P_0' to 'P_{11}' and vertical check bits 'V_0' to 'V_{15}'. The decoding process is made to navigate through syndrome calculator, error locator and error corrector. The decimal integer subtraction is employed to formulate horizontal

Syndrome bits and XOR operation is executed for formulation vertical syndrome bits. The non-zero horizontal syndrome bits indicates error detection whereas, vertical syndrome bits give the location of the error.

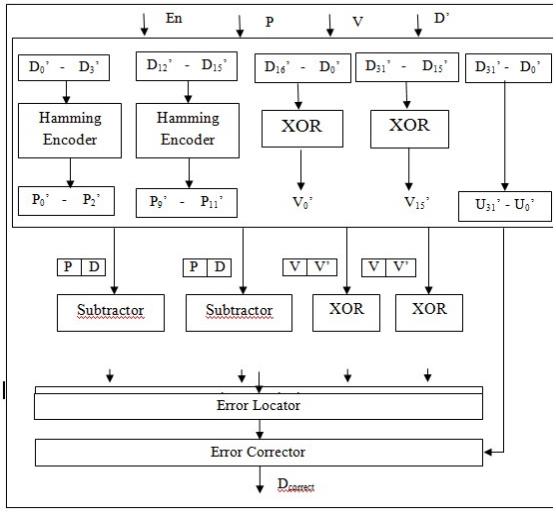

Fig.6. *Architecture of Modified DMC Decoder*

On similar lines, the back end design is carried out by using 'INNOVUS' and all performance metrics has been generated which includes area report, power report, timing report and chip layout.

The table.1 below summarizes different types of error correction capabilities of different ECC's with respect to adjacent error's. Here the length of data word considered is of 16 bit and assuming 50% of the word is erroneous. Different types of were injected which includes single as well as burst. The length of the burst is varied from 2 to 8 bits. The types of burst were chosen based on the fact that occurrence of burst of length 8bits are less frequent than that of burst error's [41-42] of length below 8 bits. And hence are injected accordingly to estimate percentage of error correction. The results presented in table.1 clearly convey the fact that the proposed ECC is capable of achieving very high correction rate, up to 5bit adjacent error and gradually deteriorates its performance for the of seven and eight bit adjacent shown in fig.7.

4. RESULTS & DISCUSSIONS

The evaluation of proposed system has been exhibited under two categories namely front end analysis and back end analysis. In front end design, the analysis is carried out by modelsim, and Xilinx. The physical design is carried out by using cadence. The functional analysis is carried out by using GENUS. The performance metrics has been generated which includes area report, power report, timing report and RTL schematic has been generated.

Table.1. Adjacent Error Correction Capabilities of the proposed technique

Codes	Double Bit Error	Triple Bit Error	Quadruple Bit Error	Quintuple Bit Error	Sextuple Bit Error	Septuple Bit Error	Octuple Bit Error
CLC	100	80	62	56	40	34	18
Matrix [32]	88	52	42	28	18	8	4
DMC [36]	100	56	48	18	8	2	2
MDMC [39]	100	58	50	20	6	2	2
FUEC QAEC [40]	100	100	100	6	2	0	0
Proposed	100	100	100	100	46	4	2

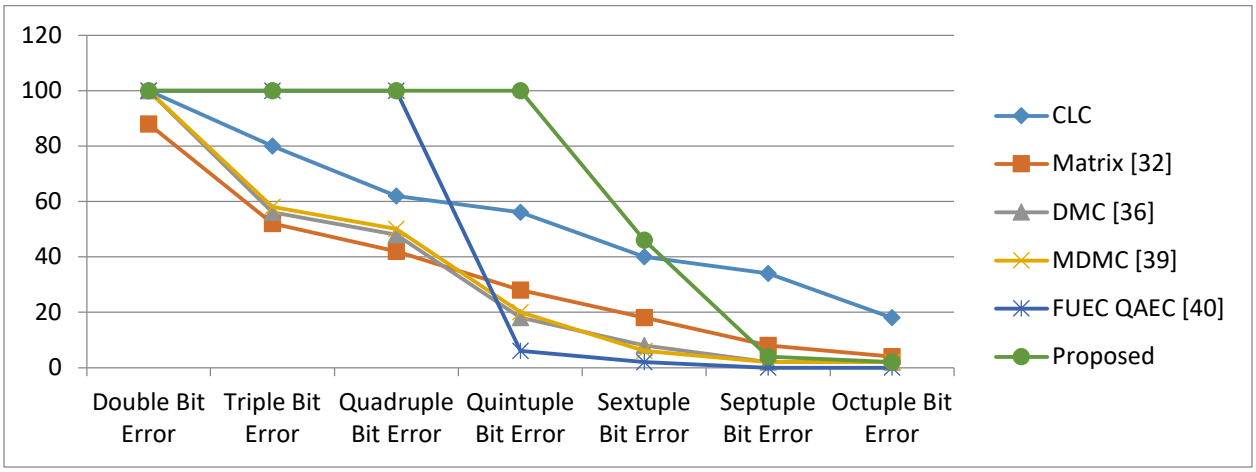

Fig.7. Comparison of Adjacent Error Correction of Different ECC's

The table.2 below summarizes different types of error correction capabilities of different ECC's with respect to random error's. The results presented in table.2 clearly convey the fact that the proposed ECC is capable of achieving very high correction rate up to 6-bit random error and gradually deteorates its performance for the of seven and eight bit random . The similar analysis is shown in fig.8. Based on the results shown in fig.7 and fig.8 it very clear that the proposed ECC's achieves very high error correction rate for both adjacent errors as well as random.

Codes	Single Bit Error	Double Bit Error	Triple Bit Error	Quadruple Bit Error	Quintuple Bit Error	Sextuple Bit Error	Septuple Bit Error	Octuple Bit Error
CLC	100	91.86	71	58	42.4	28.6	12	0
Matrix [32]	100	100	76.4	54.3	35.1	14.2	6.7	0.6
DMC [36]	100	100	100	100	100	92.6	84.7	76.0
M-DMC [39]	100	100	100	100	100	94.23	86.76	78.42
FUEC-QUAEC[40]	100	29	23.8	16.92	10	4	2	0
Proposed	100	100	100	100	100	100	80.76	68.43

Table.2. Random Error Correction Capabilities of the proposed technique

For quadruple bit, the proposed model is 45.7% superior over Matrix methodology and 83.08 superior over FUEC-QUAC methodology. The performance is elevated with sextuple bit septuple bit and octuple bit error values. For a sextuple bit, the proposed model is 71.4 % superior over CLS method, 85.8% superior over matrix method, and 98.8% superior over FUEC-QUAEC methodology. FUEC-QUAEC methodology is not fit for higher bit error values. M-DMC is almost competed which is 5.77% inferior over the proposed methodology, for septuple bit , CLC method, matrix method and FUEC-QUAEC outperforms and are not fit for higher bit error values. The proposed model is 6.91% inferior over M-DMC model for septuple bit errors. But, M-DMC model is 5.77% inferior over the proposed mode.

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ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

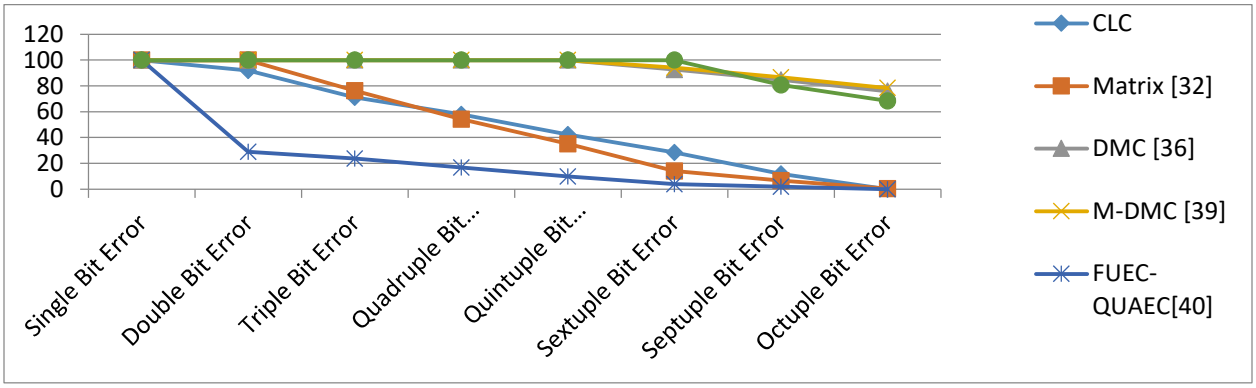

Fig.8. Comparison of Adjacent Error Correction of Different ECC's

The estimation of area, power and delay overheads has been carried out using cadence. In the front end design the parameters are estimated by using GENUS. The various performance metrics has been generated which includes area report, power report, timing report and RTL, schematic has been generated.

On Similar lines, the back end design is carried out by using INNOVUS tool and the performance metrics are generated which includes area report, power report, timing report and chip layout.

Table.3. Estimation of Hardware equivalents, Power and Area

Proposed Architecture	Area		Power				Delay (ps)
	Instant count	Total Area	Internal Power (mW)	Switching Power (mW)	Leakage Power (µW)	Total Power (mW)	
Front End Design (GENUS)	8208	49542.171	18.15	2.4	2.23	20.6 4	4
Back End Design (INNOVUS)	8277	50088.432	19.37	1.09	2.0	20.47	2.011

The table 3 presents various VLSI parameters such as area, power and delay pertaining to the proposed architecture generated by GENUS. Table 3, describes the total cell count i.e.8208 and area 49542.171nm^2 respectively. On the same lines, it can be observed that the internal power, Switching power, leakage power and total power is 18.15mW, 2,4mW, 2.23µW and 20.64 mW respectively and the total delay associated with proposed system is obtained '4'psec. Similarly, the values estimated by INNOVUS while generating chip are also presented in table3. The final gate count and final area are found to be 8277 and 50088.491respectively. The different types of powers such as internal power, switching power, leakage power and total power is found to be 19.37mW, 1.09mW, 2.0µW and 20.47mW respectively, and the total delay obtained is found to be 2.011ps. By comparing both front end design and back end design the difference in gate and total area is found to be 69 and 546.21. On same lines difference in different types of powers i.e., internal power, switching power, Leakage power and total power is found to be 1.22mW, -1.31mW, -0.23µW and -0.17. The delay difference is estimated as -1.98ps. The difference of values generated from front end and back-end design is found to be similar and are ideally be the same. The slight difference in the values is majorly due to the routing of wires for connecting the different internal components in the proposed design. The final chip design generated by INNOVUS is represented in fig.9.

Contributions made: A novel methodology is proposed to address the stated objectives. The proposed methodology is minimizing the area of the circuit, elevating the performance of the model by minimizing the power dissipation. This methodology addresses both adjacent and random errors, and eventually correction is done to improve the performance of the model. It addresses higher bit error

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ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

values up to septuple error values. DMC and M-DMC also addressed the higher bit error values, but more redundant bits are added in error detection mechanism. The proposed method overcomes the limitation with DMC and M-DMC by minimizing redundant bits with improved performance.

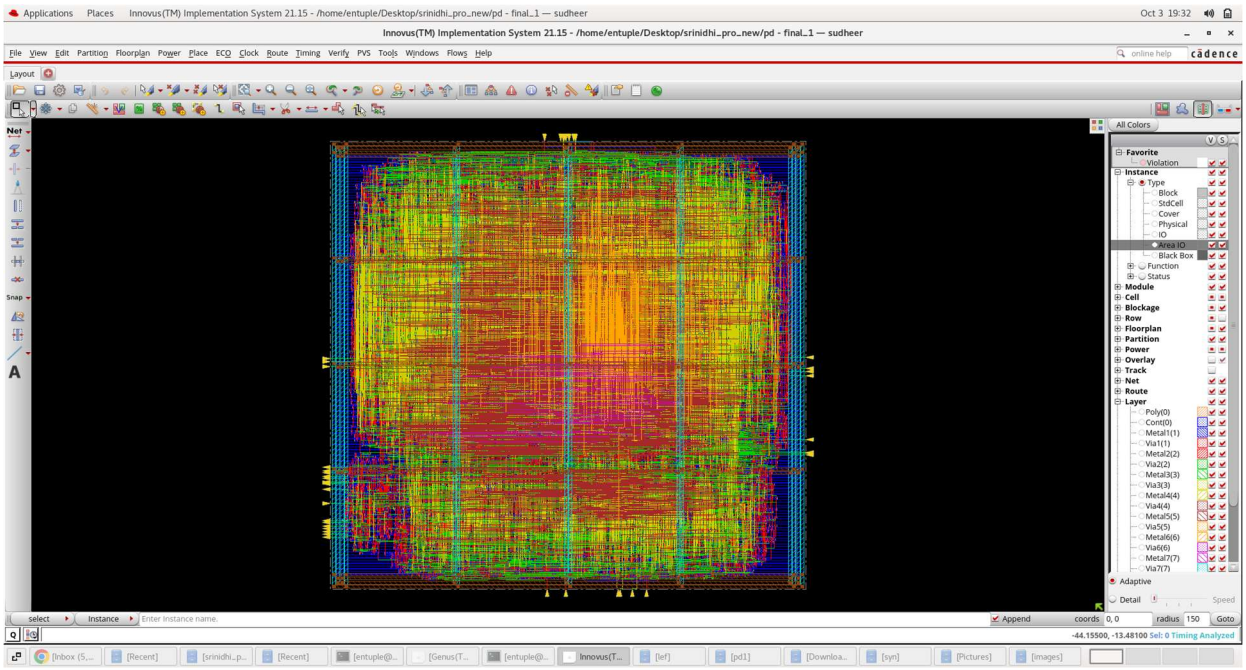

Fig.9. *Chip Layout of the Proposed Architecture*

5. CONCLUSIONS AND FUTURE SCOPE

The hybrid type error correction code is presented to ensure the reliability of SRAM memories. The proposed error correction code is obtained by integrating the inheriting properties of Modified Decimal Matrix Code and the Flexible Unequal Error Correction mechanisms, can detect single bit upsets, multiple bit upsets and as well as burst of up to 8 bits length. This can achieve 100% of error correction up to 6-bits and offers correction rate of 80.76 % and 68.43% for burst of length 7-bit and 8bit respectively. The error correction capabilities for random error is found to be 100% for Quintuple Bit Error and further, it has been observed slight decrement in error correction capability specifically for Sextuple Bit , Septuple Bit and Octuple Bit errors . This paper focused on achieving a very high error correction rate for both random and adjacent errors. The proposed error correction mechanism is significantly good for 6-bit random . It is observed that for higher bit random errors, the performance of the proposed methodology is slightly inferior. The power dissipation is due to total load capacitance of the cell i.e switching power, is estimated as 1.09mW, which is significantly a low value when compared with other error detection mechanisms. The efficiency of the proposed model is significantly improved by minimizing the power leakage to 2.0µW, which shows significant improvement in total power dissipation. The internal power is dropped to 19.37mW by minimizing the load capacitance and transition factor and mostly the voltage swing value is minimized to a significant value. Owing to minimized internal power reduction, the total efficiency of the proposed model is more reliable and efficient for real time applications. The reduction of internal power, switching power and leakage power lead to minimal total power with the proposed model. The percentage of error correction rate for Sextuple Bit , Septuple Bit and Octuple Bit are found to be 46.4 and 2 respectively. However, the increased reliability of this hybrid type error correction code is achieved at a cost of slight increment in the overhead bits. The area, power and delay overhead of the proposed architecture is found to be 50088.491, 20.7mW and 2.11ps which are very small compared to other ECC that are taken for experimental purpose and the low values of area, power and delay are mainly due to the use of encoder reuse technique. The proposed design methodology shows significantly reliable results to advance fabrication of the chip. The proposed model addressed both the

adjacent and random errors. The existing models are reasonably good for 3bit errors, but for higher bit errors, the model shows inferior performance and specifically, unable to address both adjacent and random bit error values. . These limitations are surpassed with the proposed model and significantly for 5-bit and 6-bit with improved performance.

REFERENCES:

[1] R. W. Hamming, "Error detecting and error correcting codes," *Bell Syst. Tech. J.*, vol. 29, no. 2, pp. 147–160, Apr. 1950.

[2] Alfonso Sánchez-Macián et.a;, "Hamming SEC-DAED and Extended Hamming SEC-DED-TAED Codes Through Selective Shortening and Bit Placement," in *IEEE Tran. Devices and material Reliability., Vol.14, Issue No.1, pp.574-576.*

[3]L. J. Saiz-Adalid, P. Gil, J.-C. Baraza-Calvo, J.-C. Ruiz, D. Gil-Tomas, and J. Gracia-Moran, "Modified Hamming codes to enhance short burst error detection in semiconductor memories," in *Proc. IEEE Eur. Dependable Comput. Conf. (EDCC)*, Newcastle, U.K., May 2014, pp. 62–65.

4. L. J. Saiz-Adalid, P. Gil, J.-C. Baraza-Calvo, J.-C. Ruiz, D. Gil-Tomas, and J. Gracia-Moran, "Modified Hamming codes to enhance short burst error detection in semiconductor memories," in *Proc. IEEE Eur. Dependable Comput. Conf. (EDCC)*, Newcastle, U.K.,May 2014, pp. 62–65.

[5] Wael Toghuj, "Mitigation of soft error in implantable medical devices," in *Proc. International Conference on Electrical and Electronics Engineering, April 2020, DoI: 10.1109/ICEEE49618.2020.9102553.*

I. [6] ANGELA ALVES DOS SANTOS ET.AL, "SINGLE EVENT ANALYSIS ON SRAM 180NM CMOS MEMORY WITH SUPER VOTER PROTECTION TECHNIQUE", IEEE AEROSPACE CONFERENCE, 06-13 MARCH 2021, ISSN:1095-323X, BIT SKY, MT, USA, DOI: 10.1109/AERO50100.2021.9438464

7. Helano de S. Castro, "A correction code for multiple cells upsets in memory devices for space applications", IEEE International New Circuits and Systems Conference (NEWCAS), 26-29 June 2016, Vancouver, BC, Canada, ISBN: Print: 978-1-4673-8901-3, Online: 978-1-4673-8900-6, DoI: 10.1109/NEWCAS.2016.7604783.

8. D. E. Müller, "Application of Boolean algebra to switching circuit design and to error detection," *IRE Trans. Electron. Comput.*, vol. 3, no. 3, pp. 6–12, 1954.

9. Ivan B. Djordjevic et.al, ""GLPDC Codes with Reed Muller Component Codes suitable for Optical Communications, IEEE Communications Letters, Vol.12, Issue.9, pp. 684-686, Sep-2008, ISSN No. Print: 1089-7798, Online: 1558-2558

10. Wie Yan and Sian-Jheng Lin, "Symmetric Reed Muller Codes", IEEE Trans. On Communications Vol.No. 68 Issue No.7, July 2020 pp.no. 3937-3947.

11. Wie Yan and Sian-Jheng Lin, "Local Correctabilities and Dual Codes of Symmetric Reed Muller Codes", IEEE Information Theory Work shop, IEEE International Conference 17th -21st October 2021, Kanazawa, Japan.

[12] D.C.C.FREITAS ET.AL, "ERROR COVERAGE, RELIABILITY AND COST ANALYSIS OF FAULT TOLERANCE TECHNIQUES FOR 32-BIT MEMORIES USED ON SPACE MISSIONS", 21ST IEEE SYMPOSIUM ON QUALITY ELECTRONIC DESIGN 25-26TH MARCH 2020, SANTA CLARA, CA, USA, ISSN: PRINT: 1948-3287, DOI: 10.1109/ISQED48828.2020.9137019.13. J. M. BERGER, "A NOTE ON ERROR DETECTION CODES FOR ASYMMETRIC CHANNELS," *INF. CONTROL*, VOL. 4, PP. 68–73, MAR. 1961.

[14] X. Sun et.al, "A new BIST architecture: Design and Implementation in VLSI", IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing. Proceedings, 17th-19th May 1995, ISBN: 0-7803-2553-2, Victoria, BC, Canada, DoI: 10.1109/PACRIM.1995.519568.

[15] Neagu Madalin et.al, "Unidirectional error detection, localization and correction for DRAMs: Application to on-line DRAM repair strategies", 17th IEEE International On-Line Testing Symposium, 13-15 July 2011, Athens, Greece, ISSN: Print: 1942-9398, Online: 1942-9401,

[16] Neagu Madalin et.al, "Modified berger codes for on-line DRAM repair strategies", IEEE International Conference on Automation, Quality and Testing, Robotics, 24-27 May 2012, Cluj-Napoca, Romania, ISBN: Print: 978-1-4673-0701-7, Online: 978-1-4673-0704-8.

[17] Wei-Ning Hsu, "Three-Transistor DRAM-Based Content Addressable Memory Design for Reliability and Area Efficiency", IEEE 31 31st August 2009 - 02 September 2009, International Workshop on Memory Technology, Design,

and Testing, Hsinchu, Taiwan, ISSN: 1087-4852.

18. M. Bossert, *Channel Coding for Telecommunications*. New York, NY, USA: Wiley. 1999
19. G. Neuberger, D. L. Kastensmidt, and R. Reis, "An automatic technique for optimizing Reed-Solomon codes to improve fault tolerance in memories," *IEEE Design Test Comput.*, vol. 22, no. 1, pp. 50–58, Jan.–Feb. 2005.
20. Vinod K. Malhotra, "A Double Error-Correction Scheme for Peripheral Systems", IEEE Transactions on Computers, Vol.C-25, Issue.2, pp.105-115, Feb 1976
21. Shahram Babaie et.al, "Double Bits Error Correction Using CRC Method", IEEE International conference on semantic knowledge and grid, December 2009.

[22] J.K. Wolf and D. Chun, "The single burst error detection performance of binary cyclic codes", IEEE Transactions on Communications, Vol No.42 Issue No.1, pp. 11-13, Jan 1994.

[23] Joong-Ho Lee, "Implementation in High-Speed Semiconductor Memory", 8th IEEE International Conference on Control and Automation (CA), 25-28 November 2015, Jeju, Korea (South), ISBN:978-1-5090-0397-6, DoI:10.1109/CA.2015.13.

[24] Senwen Kan, "Enhancing embedded SRAM security and error tolerance with hardware CRC and obfuscation", IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS), 12-14 October 2015, Amherst, MA, USA, ISSN: 1550-5774, DoI: 10.1109/DFT.2015.7315147

[25] Jiho Kim, Jiho Kim, "Construction of Cyclic Redundancy Check Codes for SDDC Decoding in DRAM Systems", IEEE Transactions on Circuits and Systems II, 13 May 2022, ISSN: Print: 1549-7747 Online: 1558-3791,

26. M. Zhu, L. Y. Xiao, L. L. Song, Y. J. Zhang, and H. W. Luo, "New mix codes for multiple bit upsets mitigation in fault-secure memories," *Microelectron. J.*, vol. 42, no. 3, pp. 553–561, Mar. 2011.
27. Ahmed Mohamed Mahdy et.al, "Design and Simulation of Parallel BCH Code with LDPC Code For Flash Memories", 12th IEEE International Conference on Electrical Engineering (ICEENG), 07-09 July 2020, Cairo, Egypt, ISBN: 978-1-7281-3053-8, DoI: 10.1109/ICEENG45378.2020.9171743.

[28] S. Baskar, "Error recognition and correction enhanced decoding of hybrid codes for memory application", 2nd International Conference on Devices, Circuits and Systems (ICDCS), 06-08 March 2014, Coimbatore, India, ISBN: 978-1-4799-1356-5,DoI: 10.1109/ICDCSyst.2014.6926127

[29] S. Manoj, "Improved error detection and correction for memory reliability against multiple cell upsets using DMC & PMC", IEEE Annual India Conference (INDICON), 16-18 December 2016, Bangalore, India, ISSN: 2325-9418, DoI: 10.1109/INDICON.2016.7839094

30. A. Sánchez-Macián, P. Reviriego, and J. A. Maestro, "Hamming SECDAED and extended Hamming SEC-DED-TAED codes through selective shortening and bit placement," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 1, pp. 574–576, Mar. 2014.

[31] P. Reviriego, M. Flanagan, and J. A. Maestro, "A (64,45) triple error correction code for memory applications," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 1, pp. 101–106, Mar. 2012.

32. C. Argyrides, D. K. Pradhan, and T. Kocak, "Matrix codes for reliable and cost efficient memory chips," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 3, pp. 420–428, Mar. 2011.
33. C. Argyrides, H. R. Zarandi, and D. K. Pradhan, "Matrix codes: Multiple bit upsets tolerant method for SRAM memories," in *Proc. 22nd IEEE Int. Symp. Defect Fault Tolerance VLSI Syst.*, Sep. 2007, pp. 340–348.

[34] Costas A. Argyrides, "Matrix-Based Codes for Adjacent Error Correction", IEEE Transactions on Nuclear Science, Vol. No.57 Issue No.4 ,pp.2106-2111, ISSN: Print: 0018-9499, Online: 1558-1578, DoI: 10.1109/TNS.2010.2043265.

[35] M.Priya and and M.M.Vijay "Error Detection and Correction for SRAM Systems Using Improved Redundant Matrix Code", International Conference on Recent Advances in Energy-efficient Computing and Communication (ICRAECC), 07-08 March 2019, Nagercoil, India, ISBN: Print: 978-1-5386-9483-1, Online:978-1-5386-9482-4,DoI: 10.1109/ICRAECC43874.2019.8995121

36 Jing Guo, "Enhanced Memory Reliability Against Multiple Cell Upsets Using Decimal Matrix Code", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol No.22 Issue No.2, pp 127-135 ISSN: Print: 1063-8210, Online: 1557-9999.

[37] T . Evangeline Santhia, et.al; "Error detection and correction using decimal matrix code: Survey", IEEE International Conference on

Electrical, Instrumentation and Communication Engineering (ICEICE), 27-28 April 2017, Karur, India, ISBN: Print: 978-1-5090-5921-8, Online: 978-1-5090-4996-7, DoI: 10.1109/ICEICE.2017.8191867.

[38] Naveen Kumar Yedere and Vinay Kumar Pamula, "Performance analysis of decimal matrix code and modified decimal matrix code", IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), 15-17 December 2016, Chennai, India, ISSN: 2473-943X, DoI: 10.1109/ICCIC.2016.7919617

[39] B.Shafiullah and C.Ravi Shankar Reddy, "Modified Decimal Matrix Code for Detection and Correction of Cell Up-Sets in SRAM", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE), Vol.No.4, Issue.7 2015, pp.6441-6448, ISSN: Print:2320-3765, online: 2278-8875, DOI: 10.15662/ijareeie.2015.0407096.

[40] J. Gracia-Morán, L. J. Saiz-Adalid, D. Gil-Tomás, and P. J. Gil-Vicente,``Improving error correction codes for multiple-cell upsets in space applications,"*IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2132_2142, Oct. 2018.

[41] G. I. Zebrev, K. S. Zemtsov, R. G. Useinov, M. S. Gorbunov, V. V. Emeliyanov, and A. I. Ozerov, "Multiple cell upset cross-sectionuncertainty in nanoscale memories: Microdosimetric approach," in *Proc.15th Eur. Conf. Radiat. Effects Compon. Syst. (RADECS)*, Sep. 2015,pp. 1–5.

[42] N. Chechenin and M. Sajid, "Multiple cell upsets rate estimation for 65 nm SRAM bit-cell in space radiation environment," in *Proc. 3rd Int.Conf. Exhib. Satell. Space Missions*, May 2017, p. 77.