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DESIGN OF DELAY INTERPOLATION BASED DIFFERENTIAL SELF BIASED CLOCK PLLS

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ABSTRACT

In the present day tiled and multicore processors, the traditional self biased PLL is often used with very little modification from its original architecture. The margins available for timing uncertainties, and hence the jitter constraints on the clock PLLs, have become progressively more stringent. In most of these microprocessors, the well proven architecture, the traditional self biased PLL is still being widely used with hardly any modification. The present scenario demands modifications in its topology to address the jitter constraints. This paper modifies the traditional self biased PLL targeting jitter reduction and proposes a differential self biased PLL incorporating delay interpolation based VCO that provides a constant swing VCO signal. The proposed PLL with its constant swing VCO architecture and differential PLL architecture, minimizes the input referred noise as well as the noise contribution by the VCO itself. While adopting the delay interpolation principle in the VCO of the traditional self biased PLL, it is ensured that the salient features like constant damping factor, constant loop bandwidth to reference frequency ratio, static and dynamic supply rejection characteristic is met for the entire operating frequency range of PLL and thus the proposed PLL becomes insensitive to process parameters and supply voltage variations. With a combination of delay interpolation principle and self biased scheme the modified VCO operates over a wide frequency range and hence the proposed PLL exhibits wide capture range. Detailed design followed by simulations carried out with 0.18μm CMOS process shows jitter improvement of 46% to 85% over a capture range of 1.7GHz.
Keywords: *Adaptive bandwidth PLL, Delay interpolator VCO, Jitter, Microprocessor clock, Self biased PLL.*

1. INTRODUCTION

The self biased adaptive bandwidth PLL [1] is widely employed in most of the present day tiled and multi core processors. The present day microprocessor scenario brings forth different and newer design constraints on these clock PLLs, unlike those applicable when the original traditional self biased PLL was proposed. The clock frequencies and supply voltage of these microprocessors are dynamically altered and chosen from a look up table that makes the cores operate under a predetermined power envelope [2, 3]. As these PLLs are made to operate with highest frequencies and lower supply voltages, the jitter generated from these and timing constraints also become more severe. Also, these PLLs generate clock frequencies that must be designed to switch and settle as fast as possible to newer values.

The original self biased scheme [1] primarily derives its benefits from (i) symmetric load transistors which provide both immunity against supply and process variations and, (ii) the self biased adaptive loop bandwidth nature which provides a wide operating frequency range without altering the loop stability. However, as the operating frequencies vary, the VCO swing gets progressively reduced and degrades the jitter considerably. On the other hand, the delay interpolator VCO scheme proposed in [4] operates over a wide operating frequency range with a constant swing, but without the benefits of supply noise immunity and loop bandwidth adaptivity. Moreover, this VCO also operates with differential control voltage and thus minimizes the impact of the deterministic noise generated within the circuit. The proposed work adapts the delay interpolator based VCO of [4] to the symmetric load self biased PLL scheme [1] in order to derive the benefits of both the schemes.

Though there have been many papers appearing periodically in the literature addressing

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the issue of jitter reduction in PLLs, very few of these are in the context of self biased PLLs. In [5], a delay interpolator based VCO design with low gain is proposed to minimize jitter. This design uses inverter based delay elements and hence does not meet the dynamic supply noise rejection characteristic of the proposed PLL. A calibration technique is proposed in [6] to operate the self biased adaptive bandwidth PLL with low gain VCO thereby ensuring low jitter performance. However this technique had not made use of the benefits of differential architecture. In [7], the traditional self biased PLL was modified to a dual loop scheme targeting jitter minimization addressing the issue of high gain VCO, but it requires an additional Frequency Locked Loop (FLL) circuit and digital logic circuit to control the interaction between FLL and PLL. Even though these modifications have been reported on self biased PLLs, a self biased adaptive bandwidth PLL with differential architecture employing delay interpolator VCO has not been reported.

The present paper is organized as follows. Section II explains the proposed system functionality and the adaptation of the delay interpolator VCO to the self biased PLL scheme. Detailed simulation results and overall system performance comparison with the traditional self biased PLL are presented in Section III, and the conclusions of the present work are given in Section IV.

2. ADAPTATION OF DELAY INTERPOLATOR BASED SELF BIASED VCO

The incorporation of the delay interpolation principle in the proposed PLL is explained in the following subsection. The design of proposed VCO and derivation of its gain are described in the subsequent subsection. Following that is the description of the bias generator architecture that provides the required bias voltages to the proposed VCO.

2.1 Principle of operation

The modified block diagram of the self biased PLL adopting delay interpolation principle is shown in Figure.1. The functional blocks of the proposed PLL consists of Phase Frequency Detector (PFD), charge pump circuit (CP), Loop Filters (with capacitor C and resistor R), delay interpolator VCO and prescalar. In this proposed PLL except the VCO architecture all other functional blocks remains the same as described in [1]. The modified VCO functionality is based on the delay interpolator architecture [4]. The bias generator of the delay interpolator VCO is modified from the traditional self biased VCO to derive the required bias voltages from the differential control voltages to bias the delay elements as well as the charge pump circuits.

The traditional self biased VCO with single ended control voltage is modified to delay interpolator based VCO with differential control voltage, while the salient features required for static and dynamic supply rejection characteristics of the traditional self biased PLL are preserved.

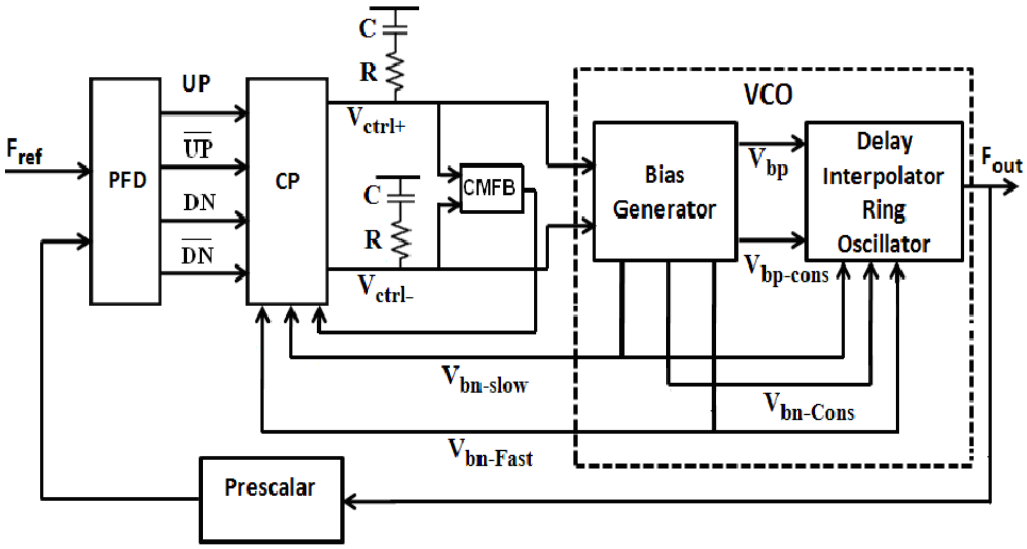

Figure 1: Block Diagram Of Self Biased PLL

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The architecture of the modified VCO is shown in Figure 2 that consists of a bias generator stage (Bias Gen) and a ring oscillator stage. The ring oscillator is designed with four delay elements.

The bias generator stage provides the appropriate bias voltages V_{bp}, V_{bp_cons}, V_{bn_cons}, V_{bn_slow}, V_{bn_fast} to the delay elements. The delay element architecture is very similar to the one employed in [4] except that the resistive load is replaced by the symmetric load proposed in [1] and this enables the resistive load of delay interpolator VCO to operate as a linear resistor for the entire frequency range of operation and hence achieves dynamic supply noise rejection. The circuit schematic of the delay element consisting of a slow path and a fast path is shown in Figure 3. As in architecture [4], the buffer stage delay in the slow path is maintained constant, independent of the control voltage whereas the inverting stage delay in the slow path is controlled by V_{bn_slow} derived from V_{ctrl-} in the bias generator. The inverting stage delay in the fast path is controlled by V_{bn_fast} generated from V_{ctrl+} in the bias generator. In the symmetric load, the current steered by V_{bn_slow} in the slow path and the current steered by V_{bn_fast} in the fast path are summed up. This summed up current I_{ss} stays constant and maintains a constant swing at the output node as in [4].

2.2 Design of modified VCO

The gain K_{VCO} of the proposed VCO is derived from the delay contributed by the individual delay element stages and is described as below.

The delay t_p contributed by a single delay element is derived from its RC equivalent model given in Figure 4, and is expressed in Eq.(1-4).

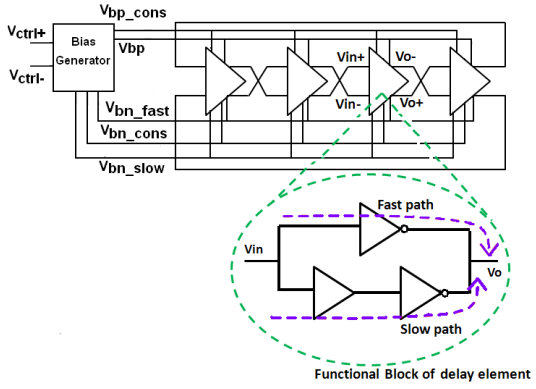

Figure 2: Functional Block Diagram Of The Proposed Self Biased VCO

$$t_p = 0.69(K_{fast}\tau_{fast} + K_{slow}\tau_{slow}). \quad (1)$$

$$K_{fast} + K_{slow} = 1 \quad (2)$$

$$\tau_{fast} = R_{fast} C_L \quad (3)$$

$$\tau_{slow} = (R_{cons} + R_{slow}) C_L + R_{cons} C_{cons} \quad (4)$$

In Eq.(1) τ_{fast}, τ_{slow} are respectively the time constants determined by the fast and slow paths. The coefficients K_{fast} and K_{slow} defined in Eq.(1) are the ratio of the current steered into slow path and fast path of the inverting stages with the total bias current I_{ss} and satisfies the relation as given in Eq.(2). In Eq.(3) the resistance R_{fast} is derived from the inverting stage in the fast path and C_L is the load capacitance at the output node of the delay element stage. In Eq.(4) R_{cons} is the resistance derived from the constant delay buffer stage in the slow path, C_{cons} is the load capacitance at the output node of the constant delay buffer in the slow path. R_{slow} is the resistance obtained from the inverting stage in the slow path.

The resistance R_{slow} and R_{fast} are derived from the symmetric load biased by V_{bp}. The resistance thus obtained is expressed in Eq.(5).

$$R_{fast}, R_{slow} = \frac{1}{2.K_p I_{ss} (V_{bp} - V_T)} \quad (5)$$

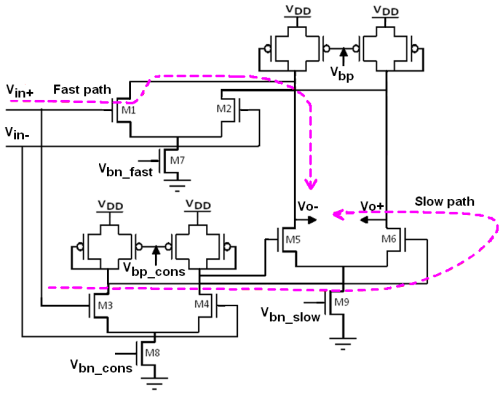

Figure 3: Functional Block Diagram Of The Proposed Self Biased VCO

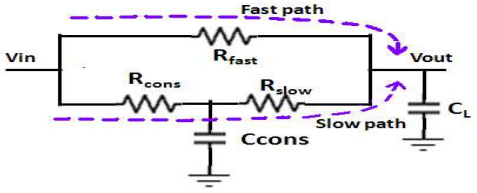

Figure 4: RC Equivalent Model Of A Single Delay Element

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Here K_p represents K′(W/L), K′ denotes process transconductance parameter and (W/L) denotes the aspect ratio of the transistors employed in the symmetric load.

The resistance R_{cons} is similarly derived from the symmetric load that is biased by V_{bp_cons}. The resistance thus obtained is expressed as

$$R_{cons} = \frac{1}{2.K_p I_{cons}(V_{bp-cons} - V_T)} \quad (6)$$

Here I_{cons} and V_{bp_cons} are derived from a constant bias voltage in the bias generator.

The VCO frequency is thus controlled by time the constants τ_{fast} and τ_{slow} and the coeffecients k_{fast} and K_{slow}. The time constants are independent of control voltage, whereas the coefficients k_{fast} and K_{slow} play the role of transconductance of the transistors steering current into the inverting stages of the slow and fast path.

Hence the K_{VCO} characteristic is nonlinear which is unlike the characteristic in traditional self biased VCO. But with the combination of delay interpolation principle and self bias principle, the VCO has the capability to exhibit wide operating frequency range very similar to the traditional self biased VCO.

2.3 Design of modified bias generator

The bias generator is designed so that it preserves the supply rejection characteristic of the traditional self biased VCO. The circuit architecture of the modified bias generator modified from [1] is shown in figure.5. The bias voltage V_{bp} required for biasing the symmetric load of slow and fast path inverting stage is generated in a half buffer replica stage, which is one half of the delay element stage similar to that adopted in [1]. The bias voltage V_{bp} generated in the replica buffer stage, is obtained by summing up the current steered by differential

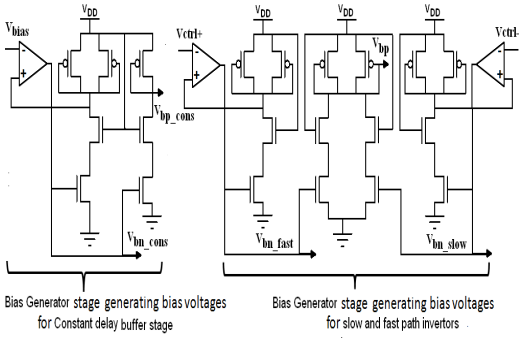

Figure 5: Circuit Schematic Of Bias Generator

voltages V_{bn_slow} and V_{bn_fast}. Therefore the voltage V_{bp} stays constant irrespective of the control voltage since the bias voltages V_{bn_slow} and V_{bn_fast} are differential. Since these bias voltages also bias the delay element stages, it ensures the lower limit of the constant swing in the delay element as V_{bp} and hence meets the dynamic supply rejection characteristic of the traditional self biased PLL. The architecture also permits the bias voltage V_{bp} to track supply voltage variations, with V_{bn_slow} and hence retains the static supply rejection characteristics of traditional self biased VCO.

3. PROPOSED PLL SYSTEM DESIGN

Design of charge pump circuit and the PLL loop parameters are explained in the following subsections. The proposed PLL loop parameters are derived similar to the technique adopted in the traditional self biased PLL and is shown that it meets the requirements of constant damping factor and adaptive bandwidth over its entire operating frequency range as in [1].

3.1 Charge Pump circuit design considerations

The architecture of charge pump circuit is shown in Figure 6, and is very similar to the architecture employed in [1]. Similar to the design consideration applied in traditional self biased PLL, the charge pump device dimensions are chosen in certain relation with the device dimensions of the VCO delay elements. This helps in minimizing the mismatch between the currents steered by the UP and DN signals in the charge pump. Thus the device dimensions in VCO and hence the charge pump circuit device dimensions are chosen in such a way that the required operating frequency range is met and also the random noise generated from the charge pump circuit is as minimum as possible.

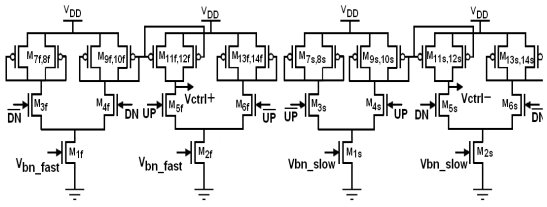

Figure 6: Architecture Of Charge Pump Circuit Generating Differential Control Voltage

3.2 Proposed PLL loop parameter description

The PLL damping factor ζ is one of the deciding factors of jitter performance in clock

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generation circuit. The damping factor of a second order PLL is given in Eq.(7).

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{cp}.K_{VCO}.C}{N}} \quad (7)$$

Charge pump current and loop filter resistance is derived from VCO's delay element bias current, very similar to the traditional self biased PLL. The expression for ζ is similarly derived and is given in Eq.(8).

$$\zeta = \frac{y}{4\sqrt{2}}\sqrt{\frac{x.K_{VCO}.C}{2.M.N}} \quad (8)$$

The factor '*x*' is defined by the ratio of the charge pump current I_{cp} to the current defined in the delay element I_{ss}. The factor '*y*' is used to define resistance R of the loop filter similar to the technique employed in [1]. Here C is the capacitance of loop filter, N is the prescalar division factor and M is a constant defined as

$$M = (0.69).2.n. \quad (9)$$

Here '*n*' is the number of delay element stages incorporated in VCO.

By approximating VCO gain characteristic to be linear, from Eq.(9), it can be seen that ζ attains a constant value for the entire frequency range of operation very similar to the condition obtained in [1].

The proposed PLL loop bandwidth is made to track the operating frequency similar to [1]. The resonant frequency ω_n for a second order PLL is expressed as given in Eq.(10).

$$\omega_n = \sqrt{\frac{x.I_{ss}.K_{VCO}}{N.C}} \quad (10)$$

The ratio of reference frequency ω_{ref} to ω_n for the proposed self biased PLL is derived similar to that in [1], using the conditions given in Eq.(11).

$$R_{cons} = z.R_{fast} = z.R_{slow..} \quad (11)$$

In Eq.(11) z is a constant. Using this condition, the derived ω_{ref} to ω_n is expressed as in Eq.(12).

$$\frac{\omega_{ref}}{\omega_n} = \frac{2\pi}{M}\sqrt{\frac{2k_p}{x.K_{VCO}}}\frac{\sqrt{C}}{C_L}\left(\frac{1}{K_{fast}+K_{slow}\left(1+z+\frac{z.C_{cons}}{C_L}\right)}\right) \quad (12)$$

The ratio ω_{ref} to ω_n is thus found to be constant dependent on ratio of capacitances approximating K_{VCO} to be a constant. Thus the system possesses adaptive bandwidth nature, independent of process variations similar to that in [1].

4. PROPOSED PLL DESIGN SPECIFICATIONS AND SIMULATION RESULTS

A traditional self biased PLL was designed to compare the jitter performance with the proposed PLL. The traditional self biased PLL was first designed with loop parameters ζ to set to be 1, and the ratio ω_{ref} to ω_n was set to be 15. Also, the traditional self biased VCO was designed with a tuning range of 800MHz to 2.7GHz. For the proposed differential self biased PLL, the VCO was designed with a similar tuning range. The charge pump bias currents, loop filter R and C values, and the prescalar value (N=16) was set to be identical for both cases. With these system parameters chosen, the proposed differential self biased PLL and the traditional self biased PLL will have identical loop parameters ζ as 1 and ω_{ref} to ω_n as 15 and hence their performance comparison is expected to be fair.

4.1 Simulation Results

Simulation results are presented for the proposed as well as the traditional self biased PLL. Circuit simulations were carried out using 0.18µm CMOS process in Cadence.

The proposed VCO's gain characteristic is shown in Figure 7. Even though the gain characteristic is observed to be nonlinear, due to the combination of delay interpolation and self bias principle, the proposed VCO exhibits a wide operating range of frequencies 850MHz to 2.7GHz.

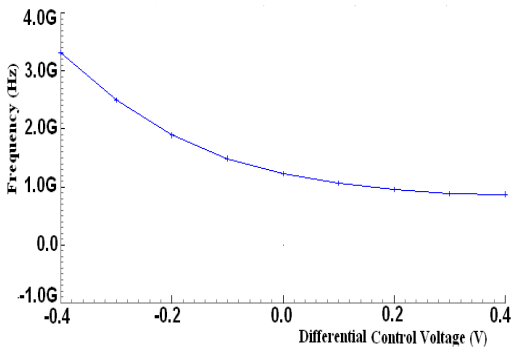

Figure 7: VCO Gain Of The Proposed Self Biased PLL

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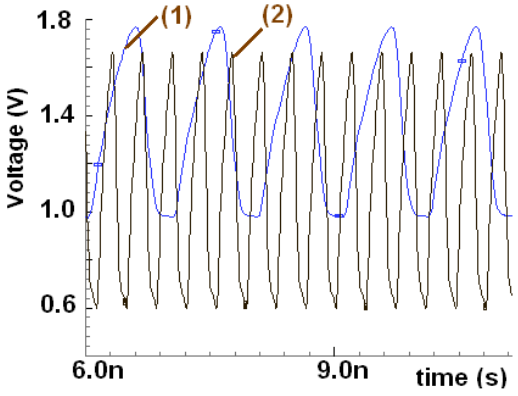

Figure 8a: Traditional Self Biased VCO Swing

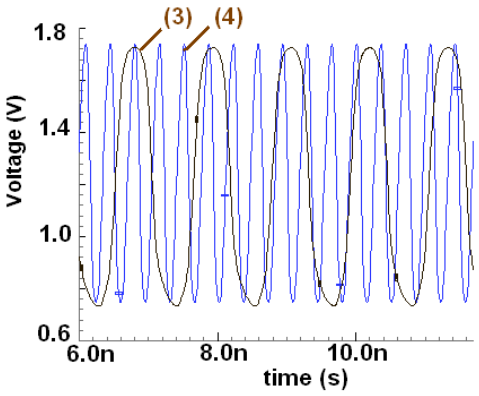

Figure 8b: Proposed Self Biased VCO Swing

Constant swing obtained from the proposed VCO is shown in comparison with the output swing obtained from the traditional VCO in Figure 8a,b. It can be seen from Figure8a. that the traditional VCO swing varies with operating frequency. At 900MHz, the VCO swing as seen from the waveform labeled (1), is observed to be 0.8V and at 2.8GHz as seen from the waveform labeled (2), it is observed to be 1.1V. The constant VCO swing retained by the proposed delay interpolator VCO is shown in Figure8b. A constant VCO swing of 1.1V is observed at the extreme frequency of 900MHz marked as (3) and at the other extreme frequency of 2.8GHz marked as (4).Thus the proposed VCO is observed to retain its swing to 1.1V over its entire operating frequencies.

The bias voltage transients of the traditional and proposed self biased PLL are shown in Figure 9 at an operating frequency of 2.1GHz. From the bias voltage transients V_{bn} of the traditional self biased PLL and V_{bn_slow} and V_{bn_fast} of the proposed PLL, it can be observed that both the system settle times are very closer. The traditional self biased PLL is observed to settle at 110ns (14 reference clock cycles) and the settling time of the proposed self biased PLL is found to be very closer at 114ns (15reference clock cycles) with a frequency step of 700MHz from the free running frequency.

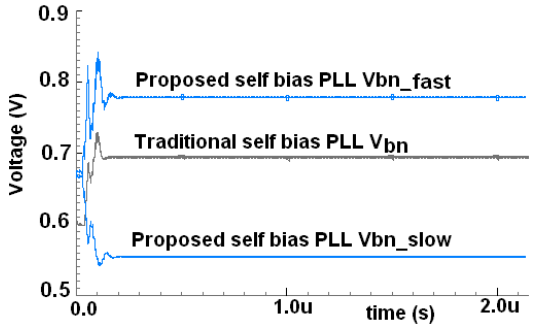

Figure 9: Capture Transients Of Bias Voltages Of The Traditional And The Proposed Self Biased PLL At 2.1ghz

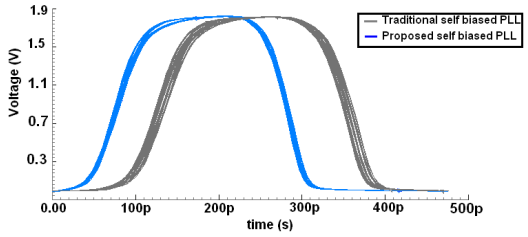

Figure 10: Jitter Performance At 2.1ghz Output Frequency

The peak to peak jitter measure using an eye diagram plot is shown in Figure 10 for the two architectures at the operating frequencies of 2.1GHz. The peak to peak jitter measure for the traditional self biased PLL architecture is 12.4ps (0.026UI) where as for the proposed self biased PLL it is observed to be 5.9ps (0.012UI), thereby the proposed PLL shows 52% improvement in jitter performance.

The proposed PLL operates over wide frequency range of 1GHz to 2.7GHz. The PLL performance at these extreme frequencies of 1GHz and 2.7GHz are tabulated in Table.1. From the table it can be noted that significant jitter performance improvement of 46% to 85% is obtained with negligible degradation in its settling time. Supply rejection characteristic is verified by simulating supply noise as a sinusoidal source of 10mV with 100MHz frequency added with the DC supply source. The observed jitter for the traditional PLL under this noisy supply is 38.6ps (0.038UI) and for the proposed PLL the jitter is observed to be 13.8ps

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(0.013UI) showing 64% improvement. There is a marginal degradation while comparing jitter performance improvement with the noiseless case of 1GHz output frequency, as the bias generator of the proposed PLL drives a larger capacitive load, hence the gain at 100MHz supply noise of the proposed PLL bias generator degrades when compared with the gain of the traditional self biased PLL bias generator.

Table 1 : Performance Comparison At Extreme Operating Frequencies

Output frequency	Performance parameter	Traditional self biased PLL	Proposed self biased PLL
1GHz	Jitter	19.6ps (0.019UI)	3ps (0.003UI)
	Settling time (frequency step of 400MHz)	210ns (13 reference clock cycles)	216ns (14 reference clock cycles)
2.7GHz	Jitter	7.9ps (0.02UI)	4.28ps (0.011UI)
	Settling time (frequency step of 1.3GHz)	135ns (23 reference clock cycles)	188ns (32 reference clock cycles)
-------	Capture range	1GHz-2.7GHz	900MHz-2.7GHz

5. CONCLUSIONS

It is demonstrated in this paper that it possible to suitably combine the traditional self biased PLL and the delay interpolator VCO in order to derive the benefits of both the schemes. The proposed PLL shows significant improvement in jitter while compared with the traditional self biased PLL without exhibiting any degradation in the settling time. Since the system bandwidth is adaptive, the proposed PLL captures over a wide frequency span of 1.7GHz. It was also observed that the proposed scheme is capable of jitter improvements ranging from 46% to 85 % with marginal degradation in the capture time and supply rejection. It was also shown that the VCO swing in the proposed PLL has a constant signal swing 1.1V over the entire operating frequency range. Further increase VCO swing might be possible and this will be taken up for future work.

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